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On the Cover…
The cover photograph is a custom Quad N-Channel MOSFET built for Cassini-Huygens Probe. After Particle Impact Noise Detection (PIND) was performed, it was found that the lids of the packages were hitting bond wires' arc apogee. (Photo and description courtesy of University of Michigan).

WWW URL Address:
http://arioch.gsfc.nasa.gov/eee_links/eeeintro.html

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LETTER FROM THE EDITOR

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Welcome to the June issue of EEE Links. Each new issue of EEE Links continues to grow in size and in diversity of articles. There are a number of new authors in this issue writing on a wide range of Parts and Packaging topics. I would like to extend a warm welcome to the new authors as well as continue to thank our authors who write columns on a regular basis. Remember, EEE Links is your " tool" to use as you see fit by submitting articles that you deem useful. Please continue to give us feedback and suggestions as to what you would like to see in the upcoming issues.

ENABLING THE EVOLUTION OF THE COMMERCIAL ELECTRONICS INDUSTRY: ADDRESSING RADIATION EFFECTS ON EMERGING TERRESTRIAL ELECTRONICS

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The commercial electronics industry, pushing the state-of-the-art component technology, has come upon an interesting obstacle in the emerging ultra high density and low voltage arena - the radiation environment on Earth presents a hazard to the reliable performance of these components. In fact, single event upsets, or soft errors, have been observed in terrestrial applications of many currently available memory technologies. Fortunately, software mitigation schemes, such as Error Detection and Correction (EDAC), may be implemented in memory storage applications. Recently, soft errors in logic has become a "hot topic" in commercial electronics reliability circles. In fact, as geometries and operating voltages continue to decrease, component sensitivity to the radiation environment is expected to increase. NASA has stepped up to provide an enabling role to commercial industry in the solution of these issues. Indeed, there exists an extensive capability within the space community to address the effects of space radiation on electronics. Space use of commercial and nonradiation-hardened electronic components has increased over the past few years, leading to the development of component testing, models, and design and mitigation technology, with the objective of eliminating the effects of such events on operational performance. The partnering of the space and commercial industries is intended to provide the capabilities, expertise, technologies, and facilities necessary for leapfrogging into the ultra high density/low voltage arena.

Collaboration between NASA and SEMATECH (Semiconductor Manufacturing Technology) consortia initiated a meeting of interested parties, held in January 1997 at NASA Goddard Space Flight Center. Attendees included: representatives from Motorola, Digital Equipment Corporation, Texas Instruments, CRAY Research, Lockheed Martin, Northrup Grumman, National Science Foundation, NASA, Jet Propulsion Laboratory, Applied Physics Laboratory, Vanderbilt University, University of New Mexico, and Prairie View A&M. This not-for-profit link between the commercial electronics and space industries allows for technical cooperation and a solution-oriented collaboration. The meeting proved extremely fruitful, and sparked the development of a symposium on the topic to allow for more technical discussion and a wider audience. SRC, Semiconductor Research Corporation, has offered to co-sponsor the symposium with NASA and SEMATECH.

The SEMATECH/NASA/SRC First Symposium of Radiation Effects in Terrestrial Electronics will be held October 27 and 28, 1997 at NASA Goddard Space Flight Center. Individuals from SEMATECH, NASA, Sandia National Laboratory, Applied Physics Laboratory, and Vanderbilt University will chair the sessions, which include: Soft Errors and Reliability, Submicron Technology Issues, Low Power Issues, Test Facilities, Embedded Applications, and Solutions for Space/Lessons Learned. Invited papers will be given by Dr. Eugene Normand, Boeing Defense & Space, and Dr. Lloyd Massengill, Vanderbilt University. Following the technical sessions, an open forum will be held to discuss the symposium, industry needs, and future collaborations. The call for presentations and announcement of the meeting will be distributed shortly via SEMATECH and SRC mailing lists and IEEE National Space Radiation Effects Conference attendee lists.

The intent of this collaboration is to bring together the space radiation effects community with commercial industry, with the ultimate benefit to industry of achieving their goals in ultra high density/low voltage. This effort also allows industry to utilize existing capabilities, technologies, expertise, and test facilities to speed technology development. The payoff of this activity to NASA is *immense*! If the commercial electronics industry produces components which are immune to some, or all, of the radiation-induced failure modes, greater reliability in both aeronautics and space applications will be achieved! In addition, the availability of ultra low voltage electronics translates directly to cost savings in space vehicle flight.

The resulting reduction in power requirements, such as battery and solar array size, and in component size for increased functionality would allow the development of much smaller and lighter space systems!

STUDY OF CONFORMAL COATING ON CHIP-ON-BOARD (COB) TECHNOLOGY FOR SPACE APPLICATIONS

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1.0 Abstract

In this faster, smaller and cheaper microelectronics world, NASA's New Millennium Program initiatives are aimed at developing miniaturized spacecraft that provide more scientific data at minimum cost. This study is aimed at evaluating coating materials that can be used in space flight applications as a die protection against the harsh space environment. NASA Goddard Space Flight Center (GSFC) as part of collaborative work with The Johns Hopkins University, Applied Physics Laboratory initiated this conformal coating study. Use of Chip-on-Board (COB) is one of the key technologies for spacecraft miniaturization. COB technology has been around for the past 20 years, and has continued to evolve in the consumer electronics market, and recently, its popularity has increased in high-reliability applications such as space flight electronics. The use of COB in military and aerospace applications will grow if reliability has been demonstrated. This conformal coating study is intended to provide reliability data for protection of bare dice in space flight.

2.0 Introduction

In COB design, there are three major COB assembly techniques, namely chip-and-wire (wire bonding), tape automated bonding (TAB), and flip-chip. Figure 1 depicts three chip level interconnects.

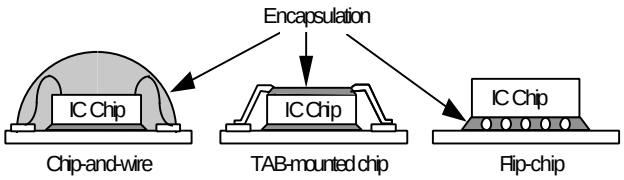

Figure 1
Schematic of Three Major COB Interconnect Techniques

Wire bonding was developed by Bell Lab in 1957, and is the most widely used technique for electrical interconnection in the microelectronics industry. This technique was chosen for this study mainly because of its advantages in supporting small volume production, and rework capability.

TAB, was conceived by GE in the late 1960s to replace wire-bonding technology. TAB offers better electrical performance due to its shorter interconnect leads within a rectangular cross-section. Because TAB requires extra wafer processing and extra tooling, its cost is higher than other techniques. This makes it more suitable for higher volume production.

In the 1960s, IBM developed flip chip technique, which is also known as controlled collapse chip connection (C4). It has a high I/O compared to wire bonding, but utilizes a high-cost material such as ceramic. C4 is difficult to rework and clean, and exhibits a high coefficient of thermal expansion (CTE) mismatch between the chip and carrier.

The user should determine appropriate interconnect techniques for their applications considering key factors such as cost, performance, and reliability. Mounting bare die directly on a board requires proper device protection to ensure long-term reliability. A good surface coating material can protect against harsh environments such as moisture, contamination, mobile ions, and radiation. Conformal coating materials require excellent electrical and mechanical properties, capable of withstanding extreme temperature cycling requirements (-55°C to 125°C) imposed on space flight electronics.

Environment factors must be considered when selecting coating materials for COB technology for space flight use. Factors such as chemical effects, zero gravity, zero pressure, plasma, and atomic oxygen should be considered prior to coating material selection.

3.0 Die Coating Materials

The preferred choice for coating material should have a high glass transition temperature (Tg ≥ 150 °C) and should have a similar CTE to that of the bond wire mate-

rial. The coating material should have excellent adhesion to the die surface to ensure the bonding between the assembly and the coating during vibration testing. In addition, since COB technology is often mixed with surface mounted technology (SMT), the material should be compatible with the soldering assembly process. Ionic contamination can severely damage the COB device and jeopardize its long-term reliability. In a presence of moisture, corrosion from ionic contamination can cause damage to the die interconnect. Selecting a material that has a low ionic contamination content (<20ppm Na^+, K^+, Cl^-) and low moisture permeability is essential. Commonly used coating materials that are compatible with COB in commercial electronic products are silicone, epoxy, silicon nitride, and parylene. Table 1 shows the advantages and disadvantages of various coating materials.

Table 1. Coating material characteristics

	Advantages	Disadvantages
Silicone	• low ionic content • low water saturation level • thermal stability • low modulus	• high CTE mismatch • low glass transition temp.
Epoxy	• low ionic content • high glass transition temp. • high elasticity modulus • comparable CTE match • excellent mechanical protection	• good adhesion characteristics coupled with their high modulus may cause encapsulant cracking
Silicon Nitride	• low moisture permeability	• high dielectric constant
Parylene-C	• chemical stability • mechanically stability • insoluble in all organic solvents • uniform coating process	• rework ability limited

4.0 Test Plan

Test sample dice with and without Silicon Nitride passivation were used in this study. Three different commercially available die encapsulant materials were used for glob-top;

1. Dexter Electronic FP4402,
2. Dexter Electronic FP4450, and
3. Dow Corning Silicone Hipec Q1-4939

To support rework, glob-top materials were only applied on the top surface of the die and not the surrounding area. This approach permits replacement of the die without damaging the bond pads on the board. The final conformal coating was applied at the board level with parylene.

4.1 Test vehicle 1: DRAM Board. The memory board depicted in figure 2 is a Chip on Board prototype assembly. This prototype is very similar to the current Command and Data Handling-C&DH In Your Palm build at the Johns Hopkins University-Applied Physics Lab (APL). This assembly consists of four stacked modules forming a 4 'by 4' by 2.5" box. Each board uses chip on board and known good die techniques. The stacked module design allows incorporation of all spacecraft bus electronics in a single stack, and allows the incorporation of additional modules. This work is being designed and built by APL in conjunction with Goddard Space Flight Center (GSFC) and the NASA EEE Parts and Packaging Programs.

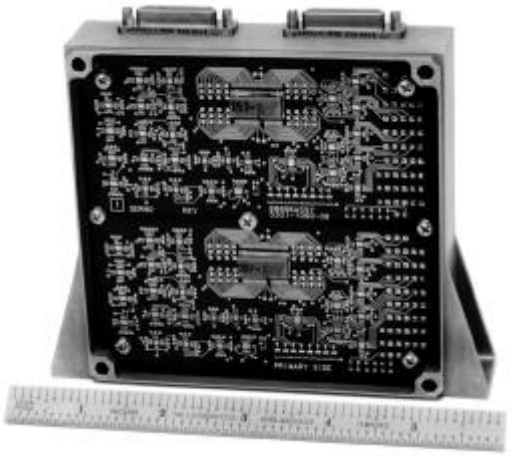

Figure 2. The DRAM Board Design with 3-D Stacked DRAMs for Conformal Coating Evaluation

A total of eleven DRAM boards were fabricated and covered with a combination of die coating materials with or without a final conformal coating. The combination of the coating materials are listed below:

Combination Items	Conformal Coating	Glob-Top	Passivation
1	Parylene	FP4402	-
2	Parylene	FP4450	-
3	Parylene	-	Si_3N_4
4	Parylene	Silicone	Si_3N_4
5	-	FP4402	Si_3N_4
6	-	FP4450	Si_3N_4
7	-	Silicone	Si_3N_4
8	Parylene	Silicone	-
9	No Coating	No Coating	No Coating

Six boards were subjected to dynamic loads test, and a temperature cycling (TC) test. The remaining five boards were exposed to temperature humidity bias (THB) test. The test conditions were as follows:

- Dynamic Load Test : Sine burst test, 50g's @35Hz, 10 cycles, Random vibration test (19.3 G's rms) 20-2000Hz, Shock test (Q=10) 100-10,000Hz
- Temperature Cycling (TC) Test : -55 °C to 125 °C for 1000 cycles
- Temperature Humidity Bias (THB) Test : 85 °C/85 % RH, for 1000 cycles, with bias voltage from -5V to 5V.

4.2 Test Vehicle 2 : Triple Track Device. The triple track device used in this test is the Assembly Test Chip, version 01 (ATC01) from Sandia National Laboratories. It is designed for use in monitoring integrated circuit damage due to corrosion of aluminum conductors. This test die contains several triple track and ladder test structures. The triple track test structures are basically very closely spaced, parallel aluminum tracks in triplets that run in a serpentine pattern. The resistance of each track can be measured and monitored for detecting corrosion. The leakage current between the tracks can also be measured to detect the presence of any conducting path formed by ionic contaminants, dendritic growths or other corrosion agents. To characterize corrosion-induced failures quantitatively, ladder structures are available. A ladder consists of a number of aluminum conductor tracks connected in parallel between two wide metal bus bars. Open paths created due to corrosion effects result in the overall ladder resistance increasing in a stepwise fashion.

Samples used in this test consisted of unpassivated parts as well as parts that have a layer of 7000 Å silicon nitride glassivation. Additional samples without any coating were also included in this test to serve as a baseline for the control samples. Two groups of tests were performed to evaluate the various die-coating materials:

1. A temperature cycling test from -55 °C to +125 °C, and
2. An 85°C /85 %RH temperature humidity biased (THB) test. During the 85°C /85 %RH THB test, the triple track structures were biased at 5V from the exterior track to the middle track and at -5V from the interior track to the middle track to accelerate the corrosion process.

A data logger unit was used to record any change in the current through the triple track devices. This enabled the detection of any changes in the die behavior. Final electrical performance of the test dice were verified using the Sentry automatic tester at intervals of 100, 250, 500, 750, and 1000 hours of the 85/85 THB test, and at 100, 250, 500, 750 and 1000 cycles of temperature cycling. Table 2 summarizes the coating materials and test matrix.

5.0 Test Results

5.1 DRAM Board Test Result. In the DRAM board test, the test results showed (Table 3) that only one combination, parylene/FP4450, passed all environmental tests. Other coating combinations could not complete a full 1000 cycles of THB.

Table 2. Triple Track Die Coating Test Matrix

Test Sample	First Coating	Second Coating	Test	Note
Un-passivated die	FP-4450	None	85°C/85 %RH THB	
Un-passivated die	FP-4450	Parylene	85°C/85 %RH THB	
Un-passivated die	FP-4402	None	85°C/85 %RH THB	
Un-passivated die	FP-4402	Parylene	85°C/85 %RH THB	
Un-passivated die	Hipec Q1-4939	None	85°C/85 %RH THB	Silicone filled
Un-passivated die	Hipec Q1-4939	Parylene	85°C/85 %RH THB	
Un-passivated die	Parylene	None	85°C/85 %RH THB	
Un-passivated die	None	None	85°C/85 %RH THB	Control sample
Die with 7000 Å glassivation	FP-4450	Parylene	85°C/85 %RH THB	
Die with 7000 Å glassivation	FP-4402	Parylene	85°C/85 %RH THB	
Die with 7000 Å glassivation	Hipec Q1-4939	Parylene	85°C/85 %RH THB	
Die with 7000 Å glassivation	Parylene	None	85°C/85 %RH THB	
Die with 7000 Å glassivation	None	None	85°C/85 %RH THB	Control sample
Die with 7000 Å glassivation	FP-4402	Parylene	-55 °C to +125 °C	
Die with 7000 Å glassivation	Hipec Q1-4939	Parylene	-55 °C to +125 °C	
Die with 7000 Å glassivation	Hipec Q1-4939	Parylene	-55 °C to +125 °C	

Table 3. Environmental testing result of DRAM boards

	6 boards		5 boards
1st ctg/2nd ctg	Vibration Test	TC Test	THB Test
Parylene/FP4402	Passed	Some Failed	Passed
Parylene/FP4450	Passed	Passed	Passed
Parylene/Si_3N_4	Passed	Passed	Failed
Parylene/Silicone/ Si_3N_4	Passed	Failed	N/A
FP4402/ Si_3N_4	N/A	N/A	Passed
FP4450/ Si_3N_4	Passed	Passed	Failed
Silicone/ Si_3N_4	N/A	N/A	Failed
Parylene/Silicone	Passed	Failed	Passed
No Coating	N/A	N/A	Failed

5.2 Triple Track Test Result. Final results from the Triple Track temperature cycling test indicate that all coating combinations with Hysol epoxies successfully passed 1000 cycles. This was not the case for the silicone-coated die, where, high thermal stresses resulting from the CTE mismatch between the encapsulant and the wire bonds caused some wire bond failures. Open circuits

started to occur at 250 cycles and the number of wire bonds that failed increased as the test progressed. Table 4 summarizes the test results and Figure 3 shows a broken wire bond in the heat affected zone on a silicone coated die.

Table 4. Triple Track Temperature Cycling Test Results

Die Coating	100 Cycles	250 Cycles	500 Cycles	750 Cycles	1000 Cycles
FP-4402	Passed	Passed	Passed	Passed	Passed
FP-4450	Passed	Passed	Passed	Passed	Passed
Silicone	Passed	17% Failed	57% Failed	81% Failed	86% Failed

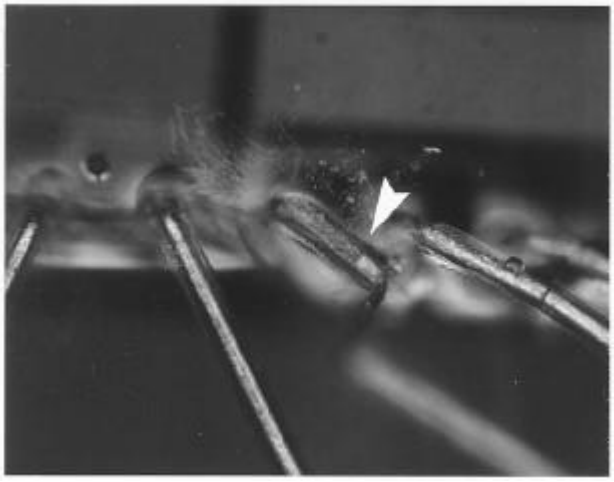

Figure 3. Photograph of a Broken Wire Bond on a Silicone Coated Die

In the 85 °C /85 %RH THB test, for samples without the manufacturer-deposited passivation, all but one die coating material (FP4402/parylene) exhibited corrosion-related failures. The control samples that did not have any encapsulant protection completely failed shortly after the test started. For dice pre-passivated with silicon nitride at the IC manufacture, all samples coated with Hysol FP4402, FP4450, silicone HIPEC Q14939, or parylene completed the 1000 hour test without any problem. The control samples without encapsulant failed starting at 250 hours. Details of the test results are included in Table 5.

Table 5. 85^0C/85 %RH THB Test Results for Samples with Passivation

Die Coating	250 Hr	500 Hr	750 Hr	1000 Hr
Hysol FP-4402/ Parylene	Passed	Passed	Passed	Passed
Hysol FP-4450/ Parylene	Passed	Passed	Passed	Passed
HIPEC Q1-4939/ Parylene	Passed	Passed	Passed	Passed
Parylene	Passed	Passed	Passed	Passed
No Coating	44% Failed	44% Failed	46% Failed	75% Failed

6.0 Conclusion

This COB conformal coating study has shown that reliability without hermeticity is achievable using commercially available encapsulant materials. COB technology together with advanced plastic encapsulated micro-electronics provides a viable packaging approach to meet the demand for "*better, faster, cheaper, and smaller"* spaceborne electronics. This research clearly demonstrated that the parylene and epoxy FP4450 combination should be the most reliable die coating material of the nine combinations tested. This study has shown that COB technology could be flight qualified with an appropriate coating employed for environmental and handling protection.

The cooperative effort between JHU/APL and GSFC, along with funding from NASA Headquarters Code Q, has made these activities possible through the joint JPL/GSFC Advanced Interconnect Technology Program. If you have any questions, comments, and suggestions, please contact Binh Le at (301)953-6000 ext. 4711, or send an e-mail to binh.le@jhuapl.edu.

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PIND TESTING REVEALS AN UNUSUAL ANOMALY IN A QUAD MOSFET

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An anomaly was noted in a course of Destructive Physical Analysis(DPA) performed on custom Quad N-Channel MOSFETS (Fig. 1) built for Cassini - Huygens Probe. One sample lot consisting of five randomly selected devices was submitted for (DPA) in accordance with S-311-M-70 and applicable Military Standards. Particle Impact Noise Detection (PIND) was performed and a detection was noted in all five samples. Devices were subsequently delidded and it was revealed that the detection resulted from the flexing lid hitting bond wires' arc apogee (Fig. 2). Due to the cost of these parts built with Harris radiation-hard dies, a decision was made to salvage the rest of this lot for the purpose of spares, by having parts equipped with newly designed "domed" lids. The new lids provide additional rigidity along with a gap increase between the underside of the lid and top of the wire arc. Lots with new lids successfully passed DPA and PIND testing. However, because of rework and additional testing and handling this lot hasn't been flown and was classified as "flight spare".

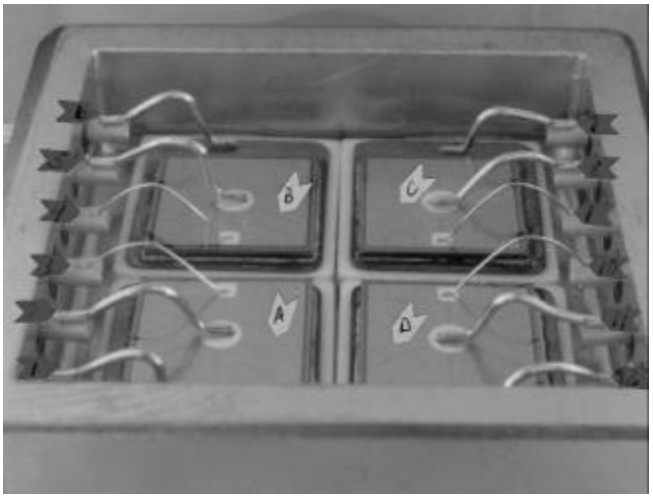

Figure 1. Quad N-Channel MOSFET
Overall view of device, Cavity Exposed

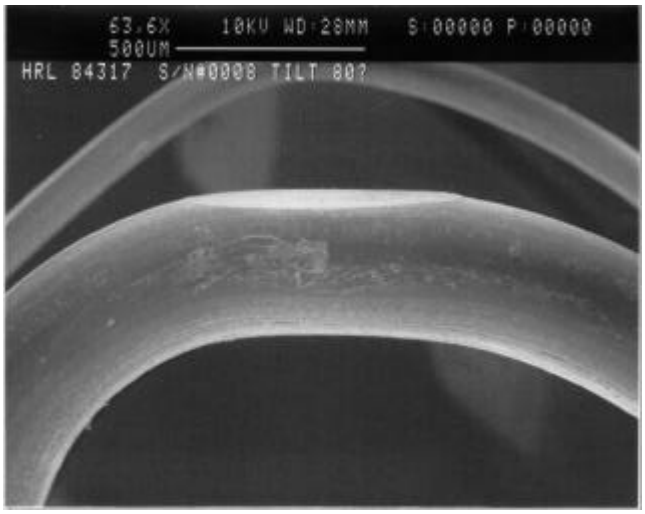

Figure 2. SEM Micrograph of flat at top of wire loop. Induced while performing pind.

ATOMIC OXYGEN AND SPACE ENVIRONMENT EFFECTS ON AEROSPACE MATERIALS FLOWN WITH EOIM-III EXPERIMENT

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Code 313

Polymer material samples mounted on a passive carrier tray were flown aboard the STS-46 Atlantis shuttle as complement to the EOIM-III (Evaluation of Oxygen Interaction with Materials) experiment. The purpose of this experiment was to evaluate the effect of atomic oxygen on the materials and to measure the gaseous shuttle bay environment. The morpho-logical changes of the samples produced by the atomic oxygen fluence of 2.07E-20 atoms/cm^2 are reported. The changes have been verified using Electron Spectroscopy for Chemical Analysis (ESCA), gravimetric measurement, microscopic observations and thermo-optical measurements. The samples, including Kapton, Delrin, epoxies, Beta Cloth,

Chemglaze Z306, silver Teflon, silicone coatings, 3M tape and Uralane and Ultem, PEEK, Victrex (PES), Polyethersulfone and Poly-methylpentene thermoplastic, were characterized by their oxygen reaction efficiency on the basis of their erosion losses and the oxygen fluence. The efficiencies shown in the table have been compared to results from other experiments, when available. The efficiencies of the samples are all in the range of E-24 g/atom. The results indicate that the reaction efficiencies of the reported materials can be grouped in about three ranges of values. The least affected materials which have efficiencies varying from 1 to 10 E-25 g/atom, include silicones, epoxies, Uralane and Teflon.

A second group with efficiency from 10 to 45 E-25 g/atom includes additional silicone coatings, Chemglaze Z306 paint and Kapton. The third range from 50 to 75 E-25 includes organic compound such as Pentene, Peek, Ultem, Sulfone and a 3M tape. A Delrin sample had the highest reaction efficiency of 179 E-25 g/atom. Two samples, the aluminum Beta cloth X389-7 and the epoxy fiberglass G-11 nonflame retardant, showed a slight mass increase.

The Atlantis Shuttle STS Mission 46, of July/August 1992, carried in orbit a large number of experiments collectively grouped under the designation of Evaluation of Oxygen Interaction with Materials (EOIM-III)—third phase. The experiments had been designed:(1) to provide atomic oxygen reactivity measurements;(2) to understand its reaction mechanism and dynamics; and (3) to characterize the induced environment in the shuttle bay.

The tray carrying the materials included 49 samples prepared by the Materials Engineering Branch, 27 by GE-Astro, 4 by IITRI and 2 by Martin Marietta. The samples consisted of thermal control paints, films, coatings and other assembly and construction materials. Of the 49 samples, the results of 9 film samples were reported in NASA document TM-104621. The results of the samples indicated above are reported in NASA TM-104636. The analyses were carried out to evaluate the effect that the oxygen flux, in conjunction with UV radiation, ionizing radiation, thermal cycling, plasma interaction and micro-meteroid/debris, have on materials used in or proposed for space applications. These types of environments, especially Atomic Oxygen (ATOX) modified by orbit altitude, spacecraft inclination and by instruments' orientation, have been shown by many flight experiments to degrade materials and S/C performances. The characterization of those effects consists of the evaluation of the exposed material thermo-optical properties, its surface erosion and/or the rates of changes of those parameters. A full report on the samples, the experiment arrangement, the results of the ground analyses and the conclusions from the experiment are reported in NASA-104636.

Material	Reaction Rate Based On Total Sample Area g/Atom	Reaction Rate Based on Exposed Area g/Atom	THERMO -OPTICAL PROPERTIES					Density
			Reflect-ance	Absorp . (Before)	Absorp. (After)	%Δ Absorp (4)	Emittance (1)	g/cm^3 (approx.) (3)
CV-2500 Silicone on Silver Coated Teflon	1.561 E-26	1.132 E-25	Fig. 15	0.692	0.714	3.18	885-NA	1.04
X389-7 Beta Cloth on Aluminum Backing	1.004 E-25	1.549 E-25	Fig. 29	0.277	0.281	1.44	0.873-0.906	—
Teflon with Ag Coated Backing	1.779 E-25	2.741 E-25	Fig. 17	0.065	0.112	—	0.793-0.808	—
Uralane 5753 LV-A/B	1.862 E-25	2.860 E-25	Fig. 49	0.612	0.651	6.37	0.880-0.912	1.0
CV-1144-0 Silicone on X389-7 Beta Cloth	2.033 E-25	3.158 E-25	Fig. 31	0.410	0.459	11.9	0.908-0.922	1.01
Epoxy Fiberglass, G-11, Flame Retardant	3.892 E-25	5.958 E-25	Fig. 9	0.643	0.657	2.17	0.906-0.903	—
Uralane 5750 LV-A/B	5.734 E-25	8.818 E-25	Fig. 47	0.558	0.648	16.12	0.843-0.878	0.96
CV-1144-0 Silicone on Silver Coated Teflon	6.427 E-25	9.831 E-25	Fig. 13	0.730	0.749	2.60	0.896-0.909	1.01
Epon 828/Versamide 140/$Ti0_2$	6.382 E-25	9.831 E-25	Fig. 51	0.212	0.289	36.3	0.905-0.898	—
CV-1142 Silicone Coating on Aluminum	8.432 E-25	1.299 E-24	Fig. 23	0.564	0.592	4.96	0.888-0.998	1.12
Chem Glaze Z-306 Black Paint	1.260 E-24	1.978 E-24	Fig. 33	0.959	0.981	2.29	0.912-0.914	0.95
CV-2500 Silicone on Kapton-H Film	1.162 E-24	1.805 E-24	Fig. 39	0.661	0.655	-0.90	0.921-0.914	1.04
CV-1500 Black Silicone on Aluminum	1.204 E-24	2.234 E-24	Fig. 25	0.931	0.927	-0.43	0.880-NA	1.24
CV-2566 Red Silicone on Aluminum	1.454 E-24	2.240 E-24	Fig. 27	0.679	0.695	2.35	0.899-0.904	1.50
CV-2500 Silicone on Delrin II 900 NC	1.508 E-24	2.276 E-24	Fig. 5	0.394	0.466	18.27	0.929-0.920	1.04
CV-1144-0 Clear Silicone Coating on Kapton-H Film	1.727 E-24	2.657 E-24	Fig. 21	0.758	0.769	1.45	0.882-0.914	1.01
CV-1144 Silicone on Delrin II 900 NC (2)	+2.896 E-24	+4.355 E-24	Fig. 3	0.401	0.492	22.6	0.926-0.912	1.01
Polymethylpentene (TPX) Film	3.247 E-24	5.011 E-24	Fig. 43	0.489	0.540	10.42	0.856-0.873	0.83
Polyethersulfone 4800 G (PES)	3.622 E-24	5.607 E-24	Fig. 41	0.539	0.619	16.35	0.889-0.895	1.37
PEEK 450 G	3.732 E-24	5.785 E-24	Fig. 37	0.617	0.681	12.96	0.880-0.894	1.26-1.32
3M Pressure Sensitive Tape No. 5	4.108 E-24	6.328 E-24	Fig. 45	0.434	0.523	20.50	0.735-0.751	—
Ultem–1000	4.454 E-24	6.894 E-24	Fig. 33	0.596	0.659	10.57	0.897-0.899	1.27
Delrin II 900	1.198 E-23	1.790 E-23	Fig. 7	0.384	0.403	4.94	0.910-0.895	—
Silver Coated Teflon with Center Hole Cut-out	7.761 E-24	1.189 E-23	Fig. 19	0.550	0.546	0.72	0.059-0.062	—
Aluminum Beta Cloth X389-7 (Aluminized Exposed) (2)	+4.605 E-26	+7.150 E-26	Fig. 53	0.263	0.266	1.14	0.125-0.125	—
Epoxy Fiberglass G11, No Flame Retardant (2)	+2.665 E-24	+4.023 E-24	Fig. 11	0.692	0.720	4.04	0.910-0.908	1.7

NOTES FOR TABLE

Fluence: 2.07 E20 atoms/cm^2
FLIGHT: STS-46 Atlantis
ORBIT: 228-230 km, 28° Inclination
Sample Area: 1.2449 cm^2
Sample Area: 0.8107 cm^2 (Exposed)

(1) Control Sample Emittance: The two indicated values of the control (not flight sample) were measured at different times as indicated on the reflectance plots. The samples were maintained in a clean closed container held at ambient conditions. The flight sample emittance could not be measured because of the measuring instrument's limitations for holding the small flight samples.

(2) These samples indicated a mass increase following the flight exposure. The nature of the mass increase has not been explored. It could be attributed to increases of oxygen or contamination.

(3) The densities' values are obtained from manufactures' data or from literature. The actual values for the tested coatings may be different due to their preparations, their coating layering and/or air inclusions. They are included so that they may be used, if desired, to obtain reaction efficiency in terms of eroded volume, cm^3/atom.

(4) The percent change of the absorptance is affected by the thickness of the coating and the backing materials.

As a reference, the commonly agreed oxygen reaction rate for Kapton is 4.26×10^{-24} g/atom or 3×10^{-24} cm^3/atom.

TECHNOLOGY VALIDATION ASSURANCE

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Electronic parts and processes are being pushed to their operational limits and new technologies are emerging to miniaturize systems and optimize performance. NASA engineers need to use these new technologies to make their hardware “cheaper, better, smaller, and faster” but lack the schedules and funding required for traditional verification programs. Traditional verification programs use long term environmental, mechanical and electrical testing to understand failure modes and application limits for a given electronic part or assembly process, and to establish its reliability history. This traditional approach has not kept pace with ongoing advances in electronic part and process technology or shrinking budgets and delivery schedules. A new method, with a focus on fast cycle time and low cost, needs to be developed to verify that these technologies will meet mission requirements without increasing risk.

The purpose of Technology Validation Assurance (TVA) is to provide a short cycle, low cost approach to building in quality through design optimization, and quality and reliability analysis for critical electronic hardware. Concurrent engineering, theoretical analysis and empirical data are used to produce information about a technology’s mechanical, thermal and electrical limitations and its most likely failure mechanisms. Current and past clients of TVA have been projects managed through GSFC, and ARPA/ RELTECH (DoD, private industry and universities).

The TVA method is comprised of three main areas: structural assessment, product evaluation, and reliability modeling. Structural assessment is performed to determine if the design process ensures reliability, manufacturability, and testability. The product evaluation phase identifies potential quality problems. The reliability modeling task involves closed-form modeling and finite element analysis to predict failure mechanisms and design and processing limits.

The innovation that makes TVA successful is its focus on getting realistic product requirements defined early in hardware development, to drive part design and manufacture. This leads to flight systems that are optimum for the intended application and that can be tested very efficiently. TVA also breaks down the boundaries between the engineering functions involved and removes assurance related bottlenecks, creating team oriented methods for problem solving.

A more in depth description of TVA can be found in the March issue of Advanced Packaging. For more information and published reports see the TVA homepage at http://misspiggy.gsfc.nasa.gov/tva. The homepage provides a library database where new and current technologies are evaluated and the proper usage of these technologies are discussed. Future evaluation reports will be loaded to the internet to the TVA library so be sure to check back to find the latest updates.

ACOUSTIC INSPECTION OF COTS ICs AND TRANSISTORS

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Abstract

The acoustic microscopy information presented in this paper was gathered during assessments of COTS, ICs, AND TRANSISTORS for research and new system development programs involving both commercial and military applications. Non-destructive acoustic microscopy inspection is more cost-effective than most sectioning and is effective in detecting some anomalies invisible to X-ray. Emphasis was placed on specific acoustic microscopy inspection techniques developed during these assessments.

1. Background

1.1 An acoustic inspection of several commercial grade ICs and transistors was performed on parts intended for a specific Navy Program. Acoustic inspections are performed in three phases:

1. Initial (as received)
2. Post pre-conditioning (Temperature Cycling, Solder Reflow, etc.), and 3. Post HAST (Highly Accelerated Stress Test). The intent of this inspection is to base line each part type upon receipt, and then monitor each part for changes as the parts are processed through pre-conditioning and HAST.

1.2. At each phase, the parts were inspected with the acoustic inspection parameters initially established for each part type. ESD precautions were taken during all inspections.

1.3. The 30 MHz transducer usually provides the best image and interface resolutions for analysis and consistent repeatability. In one instance, however, the 15 MHz transducer was required to penetrate the encapsulant. Each acoustic scan (image video and set-up parameter) was saved in the memory of the acoustic microscope's personal computer. Both the image and the set of parameters for each part inspection can be recalled from this memory file.

1.4. The initial acoustic inspection was used to develop set-up parameters to provide the most useful image information regarding each part's design, construction, material condition, and consistency in mechanical structure. This set-up was then used for acoustic inspection at each phase to monitor for significant changes. Items of particular interest being die and lead frame interfaces (potential dis-bonds and delamination areas), and die/encapsulant integrity (possible fractures, voids and porosity).

2. Initial Inspections

2.1 Initial inspections revealed inconsistencies in construction between parts from the same manufacturer; delaminations and voiding in some parts as received; porosity in some parts as received; and considerable variation in design and construction of the same generic part number from different manufacturers.

3. Subsequent Inspections

3.1 To date, both the post preconditioning and HAST phases of inspection produced image changes that often suggested increases in delamination in many of the part types. The changes in images have a high correlation with subsequent sectioning investigations.

4. Summary

4.1 This acoustic inspection effort is providing insight into the variety of inconsistencies in the commercial product world. It also shows that acoustic inspection can be used to monitor product initially for potential defects and variations in construction; and, subsequently for changes in internal integrity after processing or exposure to environment stress.

JPL-LED BGA CONSORTIUM: ASSEMBLY AND RELIABILITY TEST RESULTS

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Introduction

The Jet Propulsion Laboratory led consortium with sixteen members was established in early 1995 to evaluate the quality and reliability of Ball Grid Arrays (BGAs) and to help build the infrastructure necessary for implementation of this technology in aerospace applications[1]. Diverse membership from military, commercial, academia, and infrastructure sectors allowed a concurrent engineering approach to resolve many challenging technical issues.

Nearly 200 test vehicles, each with four packages, were assembled and tested using an experimental design. The most critical variables incorporated in this experiment were package type, board material, surface finish, solder volume, and environmental condition. The packages used

for this experiment were commercially available packages with over 250 I/Os including both plastic and ceramic BGA packages.

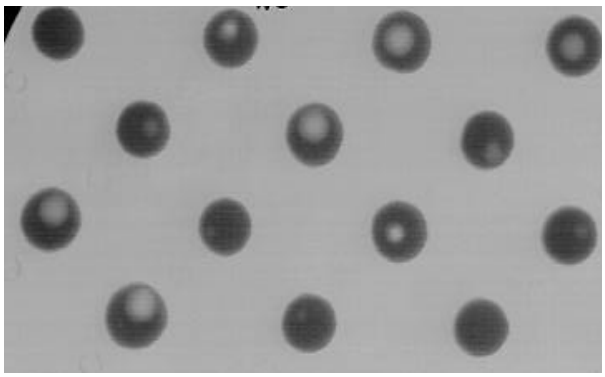
The test vehicles were subjected to thermal and dynamic environments representative of aerospace conditions. Two different thermal cycling conditions were used, the JPL cycle ranged from -30 °C to 100 °C and the Boeing and EMPF cycles ranged from -55 °C to 125 °C. Dynamic conditions simulated the launch requirements for the JPL New Millennium Project. The test vehicles were monitored continuously to detect any electrical failure. Their failure mechanisms were also characterized.

Currently, a number of plastic packages in the test vehicles have accumulated more than 3,000 JPL cycles with no solder joint failure. Extensive analysis was performed to understand failure during thermal cycling and to determine the influence and criticality of experiment variables. The test vehicles were removed periodically for optical inspection, Scanning Electron Microscopy (SEM) evaluation, and cross-sectioning for crack propagation mapping. Failure mechanisms for the two thermal environments were documented. Data collected from three facilities was analyzed and fitted to distributions using the Weibull distribution and Coffin-Manson relationships for failure projection.

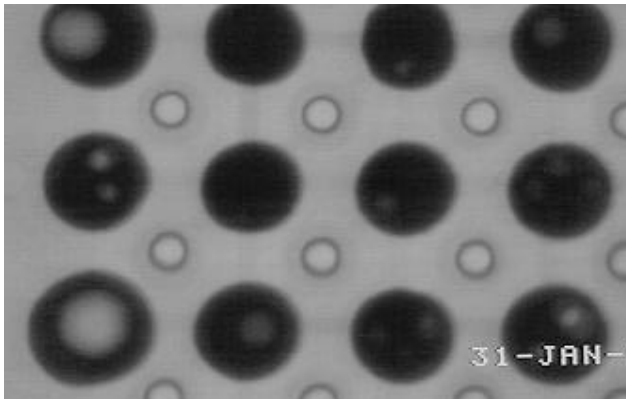
Described herein are results of process optimization including X-ray images. In addition, JPL's cycles to failure and their Weibull parameters for the 625 I/O Ceramic BGAs (CBGAs) will be compared to the results of exposure to a NASA cycle, -55°C to 100°C with a 246 minute duration.

Test Vehicle Assembling. Full assembling was implemented after process optimization from the trial test. The following materials processes were used:

- Plastic packages ranged from OMPAC to SuperBGAs and ceramic packages with 625 I/Os and 361 I/Os were used in assembling.
- Both polyimide and FR-4 PWBs with 6 layers, .062 inch thickness, were used.
- Two types of solder pastes were used, an RMA and a water soluble one.
- A 10 zone convection oven was used for reflowing.
- The first assembled Test Vehicle (TV) using an RMA reflow process was visually inspected and X-rayed to check solder joint quality.
- Interchangeability of reflow profile for RMA and Water Soluble solder pastes was examined. One TV with water soluble solder paste was reflowed using the RMA reflow profile. The solder joints showed much higher void content than expected (Figure 1), as well as signs of flux residues.
- Figure 2 shows X-ray images when an RMA reflow profile was used for the RMA solder paste. The latter showed much lower void levels rather than the large void observed in the former images.
- For water soluble paste, a new reflow profile was developed based on the manufacturer's recommendation. This reflow process was used for the remaining test vehicles.
- All fine pitch 256 QFPs had to be reworked for bridges. An X-ray example is shown in Figure 3.

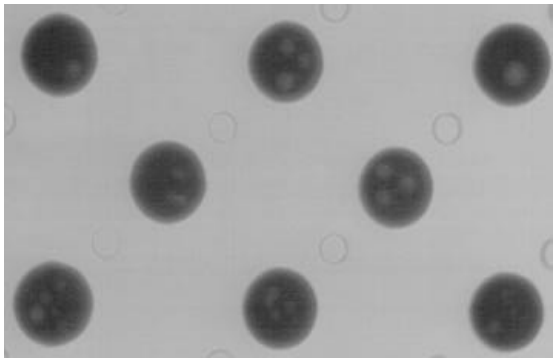


a) Excessive Voids in 313 PBGA

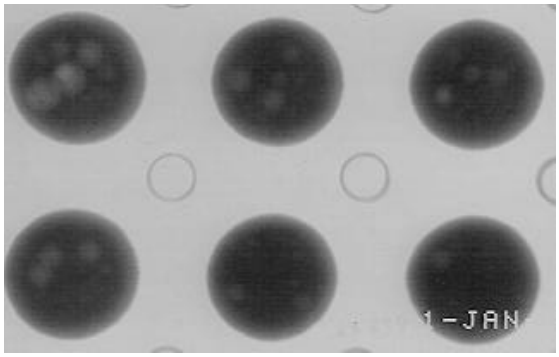


b) Excessive Voids in 352 SPBGA

Figure 1 Excessive Voids for Water Soluble with an ***RMA Reflow*** Profile



a) Reduced Voids in 313 PBGA



b) Reduced Voids in 352 SPBGA

Figure 2 Voids for Water Soluble Paste with a ***Water Soluble Reflow*** Profile

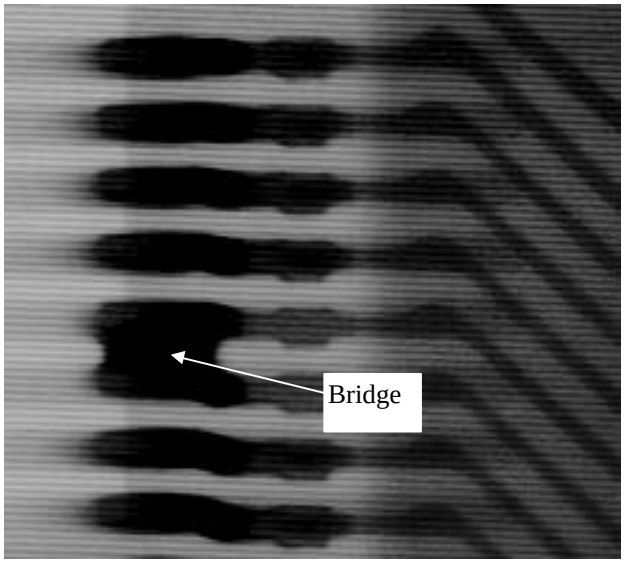


Figure 3 X-ray Photo Shows a Bridge in the 256 Fine Pitch (16 mil) QFP

BGA Thermal Cycling Results

To link our data with those of conventional SMT test results performed at JPL under another program[2]; a few TVs were subjected to a NASA cycle with a 246 minute duration.

Figure 4 compares cycles to failure for CBGA 625 I/Os and 68-, 28-, and 20-pin ceramic Leadless (LCC) assemblies subjected to this long duration cycle. For LCCs, failures were detected by Anatech® and verified by visual inspection. For this set of CBGA assemblies, failures were inspected by removing them from chamber periodically and measuring daisy chain resistances for opens.

Other BGA test vehicles were continuously monitored through a LabView system designed for this purpose[3]. The failure percentiles were approximated using a median plotting position, Fi = (i-0.3)/((n+0.4).

As expected, there was a large spread in cycles to failure for CBGAs because of variance in board materials (FR-4 and Polyimide), solder joint volume, quality and location. The first failure for CBGA was detected at 312 cycles and occurred between 292 and 312 cycles. The last failure checked at 450 cycles occurred between 439 and 450 cycles

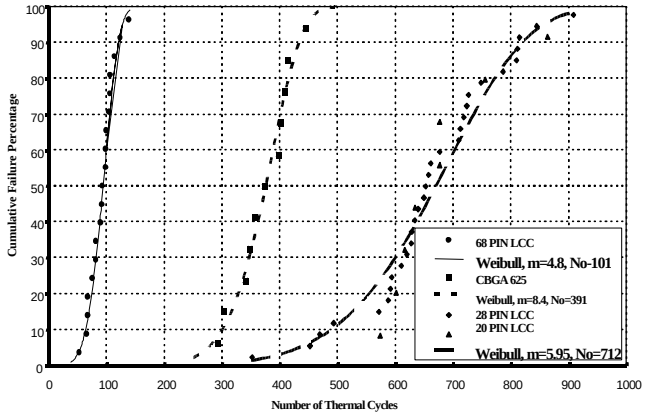


Figure 4 Cumulative Failure Distribution Plots for CBGA 625 I/O and LCC Assemblies Subjected to -55°C<->100°C with 245 minute duration

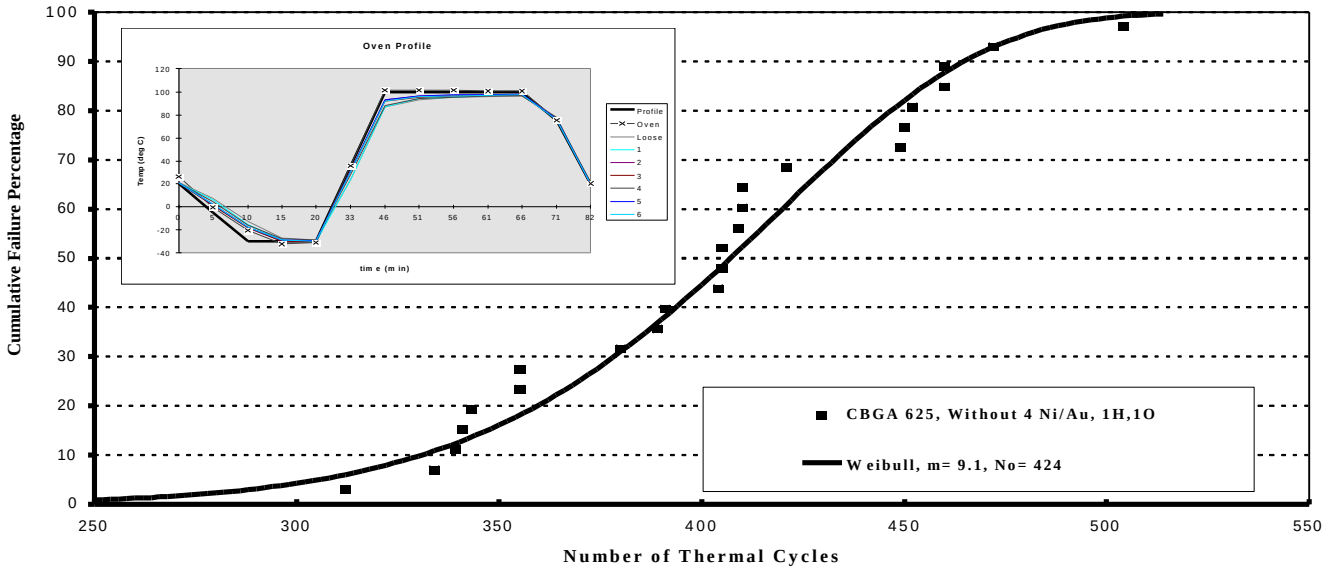


Figure 5 Cumulative Failure Distribution Plots for CBGA 625 I/O and LCC Assemblies Subjected to -30°C<->100°C with 82 minute duration

The Weibull cumulative failure distribution was used to fit cycles to failure data. The Weibull scale and shape parameters for CBGA were 391 cycles and 8.4 respectively.

Figure 5 includes cycles to failure test results for CBGA 625 I/Os assemblies on polyimide and FR-4 PWBs with different surface finishes as well as different solder volumes. These assemblies were thermally cycled between -30°C and 100°C with 82 minute duration. The thermal cycling oven temperature settings and temperature profile is also shown. Daisy chains of test vehicles were continuously monitored for failure detection. The 2P Weibull scale and shape parameters were 424 and 9.1. Five highest points, four representing those with Ni/Au and one with high solder volume, were excluded in order to get a better fit to data.

Conclusions

- The BGA void levels were the same as those generally observed by industry. As expected, BGAs were robust in assembling compared to the 256 fine pitch, 0.4 mm QFPs. All QFPs showed bridging to some degree and had to be reworked.

- RMA and water soluble reflow profiles investigated were significantly different and they should be optimized separately for the applications. A greater number of rather smaller and sporadic voids were generated when an RMA reflow profile for a water soluble solder paste was used.

- Cycles to failures for a NASA cycle (-55°C to 100°C) and a modified version used for BGA (-30°C to 100°C) did not follow a Coffin-Manson relationship. The data set showed an almost linear reduction with delta temperature (δT) rather than a near square power reduction projected by the model.

- Cycles to failure indicate that the choice of cycle selected (-30°C to 100°C) for time and cost effectiveness was appropriate.

- Cycles to failure results for the two temperature profiles are in agreement with the school of thought that suggest low temperature exposure is less critical than high temperature, and time beyond the creep threshold at high temperature has no significant effect on eutectic solder joint failure.

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[2] R. Ghaffarian, "The Interplay of Solder Joint Quality and Reliability for Leaded and Leadless Components," Ninth Annual Soldering Technology for Electronic Packaging Symposium, Oct. 21-25, 1996, Binghamton, NY

[3] K. Bonner, S. Walton, "Reliability Investigation of Ball Grid Assemblies for Space Flight Applications," Proceedings of the Technical Program, NEPCON West '97, Page 46-52

Acknowledgments

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Thanks to Sharon Walton for monitoring the environmental testing at JPL. I would like to acknowledge the in-kind contributions and cooperative efforts of BGA consortium team members including: P. Barela, K. Bonner, K. Yee, S. Bolin, C. Bodie, S. Walton, *JPL*; M. Andrews, *ITRI*; S. Lockwood, M. Simeus, P. Drake, *HMSC*; I. Sterian, B. Houghton, *Celestica*; M. Ramkumar, *RIT*; S. Levine, R. Lecesse, *Altron*; P. Mescher, *AMKOR*; Dr. N. Kim, *Boeing*; W. Goers and J. Mearig, *EMPF*; M. Cole, A. Trivedi, *IBM*; and T. Tarter, *AMD*; F. Schlieper, C. Walquist, *Nicolet*; R. Dudley, R. Balduf *View Engineering*. My deepest appreciation to others who are contributors to the progress of both programs.

ADOPTION OF INDUSTRY STANDARDS FOR ELECTRONIC FABRICATION

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An effort has been in place in the Electronic Packaging and Fabrication Section at JPL to adopt industry standards to replace internal JPL specifications. The adoption process has been extensive, involving a number of experts in the electronic packaging and fabrication areas, and also the quality area. To begin, a steering committee for the adoption of industry standards was formed. It consisted of three members from the Electronic Packaging and Fabrication organization and three members from the Quality organization. The overall electronic packaging and fabrication process was divided into 16 separate subprocesses, and a document search by subprocess was performed to identify relevant industry standards. This search led the team to consider four general document categories from which to select possible replacement documents for the JPL standards and specifications:

- NASA Handbooks (NHB)
- ANSI (American National Standards Institute) standards
- IPC (Institute for Interconnecting and Packaging Electronic Circuits) standards
- Military Standards and Specifications, provided that they had not been previously scheduled for deletion.

After the four above categories had been selected as the possible reservoir for acceptable candidate documents, various experts from both the Electronic Packaging and Fabrication organization and the Quality organization were assigned to review each subprocess. These experts also extensively reviewed pertinent candidate documents drawn from the above four sets. In some areas or subprocesses, a large number of suitable industry candidate documents existed, whereas in other areas, few suitable candidate documents were located.

Printed wiring board technology, which is a very important part of both the commercial, industrial, and military arenas, is fully documented through such organizations as the IPC. Other areas, such as polymerics and the design and fabrication of magnetic components, such as inductors and transformers, are major concerns only to the high performance/high reliability industries, as exemplified by the fabrication of spacecraft electronics. Such subprocesses have limited coverage, rendering it almost impossible to adopt non-JPL standards to cover them. One outstanding anomaly found by the committee was that of radio frequency packaging. Given that many commercial products today employ radio frequency packaging, such as cellular phones, global positioning satellite equipment, microwave communication, and satellite television, it came as a surprise that no adequate commercial/industry standards exist covering this important area of electronic packaging.

Each of the reviewers carefully studied the candidate standards for their applicability for spacecraft requirements. The chief goal of the effort was to find standards which could be directly adopted with little or no modifications for the JPL subprocesses of electronic fabrication and packaging. In the past, most of JPL’s electronic packaging and fabrication standards have been included in JPL document D-8208. This document has been the main depository for such standards. It was decided that this document should continue to serve this purpose and that Revision C should be the result of the industry standard adoption effort.

Initially, it was the goal that this document should be short, consisting mainly of paragraphs pointing to relevant industry standards identified by the experts in each subprocess of the electronic packaging and fabrication process. At the beginning of the effort, it was believed that D-8208 would point to relevant industry specifications with a very short, concise list of exceptions taken to fulfill JPL spacecraft requirements. For some subprocesses, this proved to be the case. However, for many subprocesses,

numerous exceptions were necessary because of the specific characteristics of space flight electronics.

Outgassing is a good example of the unique nature of the JPL electronic packaging problem. A major task in a space exploration mission is the photographic, ultraviolet, and infrared imaging of objects in space. All of these imaging systems have lenses which are subject to clouding if there are outgassing products generated by the electronic assemblies (or any other element of the spacecraft). This particular consideration affects many of the electronic packaging and fabrication processes, forcing numerous exceptions to industry standards. For example, cleaning of electronic assemblies to remove ionic contaminants is an important issue for high reliability. Ionic contaminants, if left on the assembly, can lead to unacceptable leakage currents and corrosion, with the possibility of total failure of the assembly. In an investigation to find suitable replacements for ozone depleting chemicals (ODCs) to comply with the dictates of the Montreal Protocol, several highly promising cleaning agents had to be rejected based solely on their unacceptable outgassing characteristics, although their cleaning performance was excellent.

Other issues complicating the adoption of standards commonly used in industry are a result of the ultra-high reliability and ultra-low volume constraints placed on space flight electronic hardware. Statistical process control (SPC) and sampling test techniques are not applicable when making one or two items which must be produced correctly the first time. This fact leads to exceptions being taken to the inspection and test procedures commonly found in industry standards.

In all, 81 industry, military, and government standards have been adopted by JPL's Electronic Packaging and Fabrication Section. However, the adoption process proved to be more difficult to implement than was first believed because of the many stringent requirements of producing space flight electronic hardware.

NONDESTRUCTIVE EVALUATION FOR MICROELECTRONIC DEVICES

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GSFC and JPL have been funded a two year (FY97 and FY98) Code Q task entitled "Nondestructive Evaluation of Structural Integrity of High-Density Electronic Packages for Space Applications". The objective of this joint task is to develop and implement applicable NDE techniques to assess joint interface integrity of high-density electronic packages and interconnects for space applications. GSFC and JPL are working in a collaborative effort, each concentrating their resources in specific areas. GSFC's effort is focused on acoustic microscopy and JPL's effort is focused on microfocus X-ray microscopy.

To date, we have performed scanning acoustic microscopy (SAM) and X-ray microscopy studies on microelectromechanical systems (MEMS) devices including tunneling accelerometers and microgyros for potential Deep Space and comet landing and take off missions. An article on the subject has been published in the March 1997 issue of EEE Links (Vol. 3, No. 1, p. 14). We have also performed tests on the joint integrity of several Ti-Pt-Au coated alumina and titanium block samples. JPL will also conduct destructive physical analysis (DPA) on the samples to correlate the SAM and X-ray results and qualify the joining process. The brazing process, if it is qualified, will be used in manufacturing of micro mass quadrapole devices.

An advantage of acoustic techniques, as compared to other NDE methods, is the ability to penetrate the material and assess its integrity (EEE Links, Vol. 2, No.2, July 1996). However, there is a trade off between the depth of penetration and resolution. Higher operating frequency has shorter wavelength, thus higher resolution. Conversely, the higher the frequency, the higher the attenuation. Since thicknesses and materials used in MEMS fabrication can vary greatly within any given device, it poses a great challenge for acoustic microscopy. The tests provide a preliminary understanding of the interaction between high-frequency acoustic waves and the devices to be evaluated. Similarly, X-ray microscopy poses a challenge for components where differences in X-ray absorption are drastically different or where thin layer of relatively transparent materials, such as silicon, are predominately used, as in MEMS. We will continue to test and determine the capabilities of SAM and X-ray microscopy for microelectronic devices.

TIME-LAPSE IMAGING OF MODIS LAMP FILAMENTS

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Moderate Resolution Imaging Spectro-radiometer (MODIS) instruments will fly on NASA's series of Earth Observing Satellites (EOS). Employing a cross-track scan mirror and collecting optics, the instrument's detectors provide imagery of the Earth's surface and cloud cover in 36 discrete spectral bands. Halogen and vacuum lamps are used to calibrate its detectors. A test to determine lamp lifetime was required to develop an instrument calibration schedule. This test was performed by the Materials Engineering Branch at Goddard Space Flight Center (GSFC). During the life test, images of the filament were periodically collected with a telescope, frame grabber, and NIH Image to record the dynamics of filament degradation. Near the end of useful life, turn-to-turn rewarding on the filament was observed and documented with more frequent image collection. This documentation graphically portrays the failure mechanism as it occurs, a significant advantage over post-test examination. For the halogen lamps, sets of time-lapse images have been stamped with time and electrical resistance and animated into a "movie". They depict the "life and death" of the filaments making it very clear when rewelding or other degradation has ruined the lamp's utility as a calibration source.

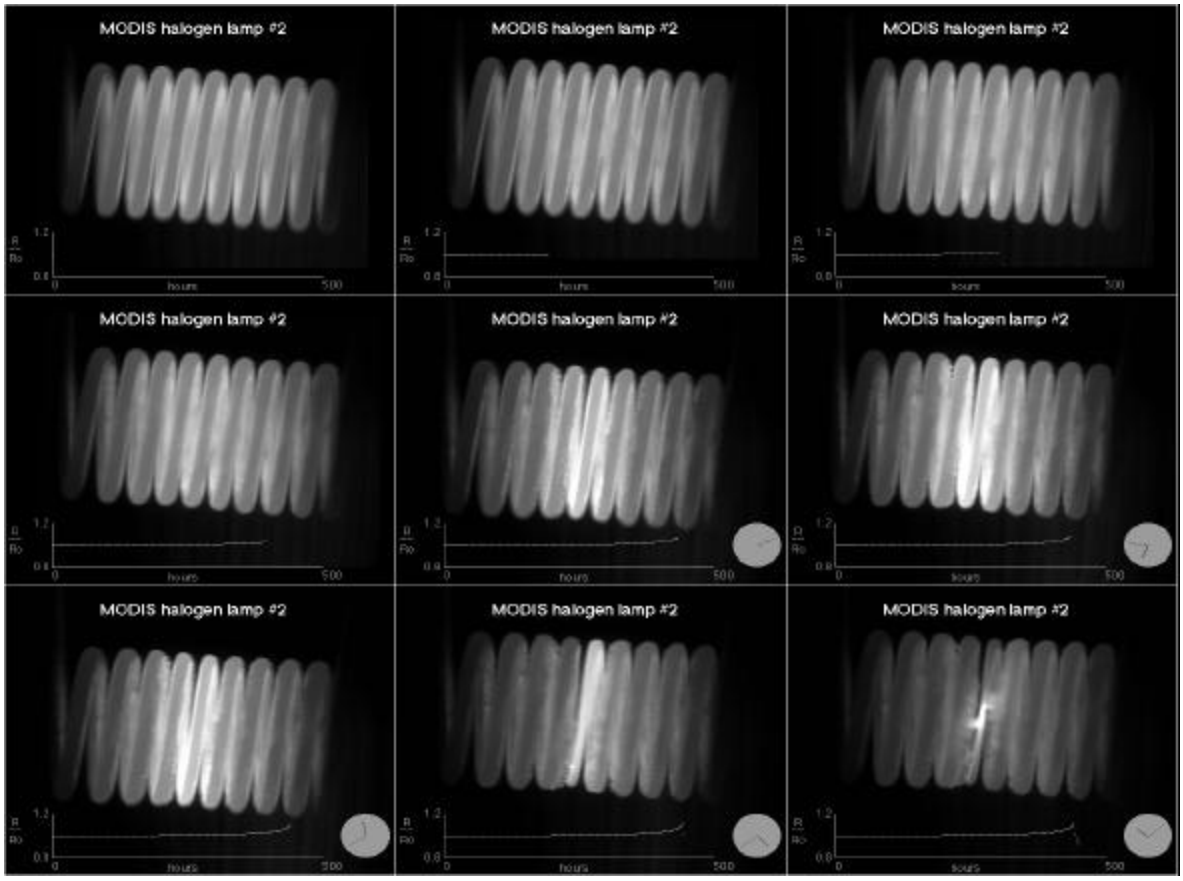

Figure 1

Figure 1 montage of filament images shows the change over time in a halogen filament during a life test. It represents a small sampling of the more than 150 images used in the complete movie. The electrical resistance of the filament vs. time (normalized to its initial resistance) is shown in the graph at the bottom of each image. As the lamps are operated with constant current, changes in resistance lead to similar changes in power dissipation. The center turn of the filament thins as tungsten evaporates and deposits on nearby turns. This leads to more abrupt increases in resistance that lead to rewelding between turns or lamp failure. The time that each image was taken can be inferred by the advance of the resistance plot and, near the end of life, by the clock face at bottom right (those images are about 5 hours apart). Halogen lamp #2 failed after 452 hours of operation when the filament opened at the hot spot shown in the lower right image.

Filament movies are available at the eSEAM virtual conference, available at: http://www.macscitech.org/eseam97/.

Mr. J. Timothy Van Sant is an electrical engineer in the Materials Engineering Branch at NASA Goddard. He has worked on the materials applications of image processing and the automation of materials testing for twelve years. He has an M.S. in Electrical Engineering from Johns Hopkins University.

Mr. Charles E. Powers also is an electrical engineer in the Materials Engineering Branch at NASA Goddard. Dating back to 1983, he has designed and built life test facilities for lamps and bearings used in Goddard spacecraft. He has also served as the materials assurance engineer for the Tropical Rainfall Measurement Mission. He has an M.S. in Physics from the American University.

Mr. Bruno F. Munoz is an electronics technician for the Unisys Corp. He has fourteen years of experience at Goddard's Office of Flight Assurance. His background includes design and fabrication of test facilities as well as considerable experience with radiographic and scanning electron microscopy.

PLATED-THROUGH-HOLE REWORK AND REPAIR

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In 1994 the Goddard Space Flight Center undertook a study entitled "How Much Rework is Too Much?: The Effects of Solder Joint Rework on Plated-Through Holes in Multilayer Printer Wiring Boards". The objective of the study was to evaluate the effects of repeated rework on solder joints and to evaluate the degradation of the plated-through-hole (PTH) structure in relationship to the board material, the soldering iron temperature, the thickness of the dielectric and the operator.

The conclusion was that for multilayer boards, it is recommended that rework be limited to three cycles. By limiting the number of reworks, the risk of inducing failure mechanisms into Printed Wiring Assemblies (PWAs) is dramatically reduced. It has long been known increasing rework cycles increases the risk of damage to the PTH and laminate, however when rework must be performed it must be done in a manner that will not introduce further damage to the PWA. Proper training of personnel performing rework is key to the success of the process.

The NASA Training Center offers a 40-hour class in Rework and Repair of PWAs. Some of the topics covered include removal of conformal coating, removing and replacing components, adding jumper wires, repairing circuit traces, isolating circuits and much more. The class is a "hands on" class. Each student works with three sample boards and then must complete a final board from instructions similar to a production situation. The students must also inspect a completed assembly for conformance to specifications.

To learn more about this class or any of the other many classes offered, call the Training Center at (301) 731-8632, or visit our Web page at **http://arioch.gsfc.nasa.gov/312/ train.htm**

UPDATE ON A/D EVALUATION AT JPL

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The following table provides a brief description of evaluations recently completed, in progress or planned for Analog to Digital converters. The evaluations include construction analysis (CA), single event latch-up (SEL) susceptibility, and total ionizing dose (TID) test. The evaluation pass/fail is relative to the intended application. The efforts are being funded by RTOP and JPL projects.

MFR	P/N 9/, 10/	Process	CA	SEL 1/	TID	Comments
Datel	ADS 937	Hybrid	Passed	8/97	See note 2/	
Linear Tech	LTC 1419	CMOS	Passed	In Process	See note 2/	
ADI	ADI 9871XE	RBCMOS	Passed	No Latch-up See note 3/	See note 4/	See note 5/
National	ADC 12062	CMOS	Not Planned	LET=12	Not Planned	
Maxim	MAX 101	Bipolar	Passed	Destructively Failed	Not Planned	
SPT	SPT 7725	Bipolar	Passed	No Latch-up, LET>100	>100krads, see note 6/	
Harris	HI 1276	Bipolar	TBD	No Latch-up, LET>100	TBD	
Harris	HI 7190	CMOS	TBD	8/97	See note 2/	
ADI	AD 7714-5, AD 7714-3	CMOS	In Process (on 7714-3)	6/97 (on 7714-3)	See note 2/	
Burr-Brown	ADS 1210	CMOS	TBD	8/97	See note 2/	
Burr-Brown	ADS 7809	CMOS	Passed See note 7/	LET=19.9 See note 7/	10krads See note 7/	See note 8/

Notes:

1/ LET expressed in MeV/mg/sq cm.

2/ Exploring supplier collaboration for TID.

3/ Work done by NSWC (Naval Surface Warfare Center, Crane Division) in collaboration with ADI.

4/ Low dose rate and temperature characterization are in progress.

5/ Rad-hard version of AD 871.

6/ Tested to 100krads with minimal degradation. The test was done with supplier collaboration.

7/ Work done by Space Electronics, Inc. (SEI) for JPL.

8/ The 7809 die along with latch-up protection circuit will be packaged in a radpak package by SEI. The reliability tests are planned as well.

9/ Expected evaluation completion date: 9/97 (except the ADS7809 which will be completed in FY 98)

10/ See section below for a brief description of each device.

Brief description of parts in evaluation

The parts being evaluated can be broken down into four distinct groups:

(a) High-speed, low power A/Ds

Datel ADS 937 16-bit, 1MHz, 1.1W hybrid A/D. The ADS 937 is a 16-bit, 1MHz sampling A/D. It is built as a hybrid and contains a sample and hold amplifier, an internal reference, timing/control logic, and error correction circuitry. It accepts both bipolar (+/-5V) and unipolar (0-10V) analog inputs. It runs on +/-5V and +/-15V power supplies and typically draws 1.1watts. The device is available in both commercial and military grades.

Linear Technology LTC1419 14-bit 800ksps, 150mW CMOS A/D. The LTC1419 is a 14-bit, 800ksps sampling A/D. It runs on +/-5V supplies and typically draws 150mW (7mW in nap mode, 10uW in sleep mode). It is available in 28-pin SO and SSOP packages.

ADI AD 9871XE 12-bit, 5MSPS, 1W radiation-hardened BiCMOS A/D. This is the radiation hardened version of AD871 12-bit 5 Msps monolithic A/D. It should be noted that the AD 9871XE is not available as a standard product (ADI made a special run for JPL). Contact the author for details.

NSC ADS 12062 12-bit, 1MHz, 75mW CMOS A/D. Using an innovative multistep conversion technique, the 12-bit ADC12062 CMOS A/D digitizes signals at a 1MHz sampling rate while consuming a maximum of only 75mW on a single +5V supply. When the converter is not digitizing signals, it can be placed in the Standby mode; typical power consumption in this mode is 100uW. It is available in 44-pin plastic leaded chip carrier and plastic quad flat pack packages.

(b) Ultra high speed A/Ds

Maxim MAX101 8-bit 500Msps, 7.5W bipolar A/D. The MAX101 is a 500Msps 8-bit A/D which allows accurate digitizing of analog signals from DC to 250MHz. Designed with Maxim's proprietary advanced bipolar processes, the MAX101 contains a high-performance T/H amplifier and two quantizers in an 84-pin ceramic flat pack. It runs on +5V and –5.2V supplies and typically draws 7.5W power. The device uses COB (chip-on-board) technology.

Signal Processing Technologies SPT 7725 8-bit 300Msps, 2.2W bipolar A/D. The SPT7725 is a monolithic (ECL) 8-bit flash converter. It operates at 300 Msps conversion rate. A single –5.2V supply is re-

quired for operation. The typical power dissipation is 2.2W. The military version of the part is available in 42 lead ceramic side brazed DIP and 44 lead surface-mount cerquad packages.

Harris HI 1276 8-bit 500Msps, 2.8W bipolar A/D. The HI1276 is an 8-bit ultra high speed flash A/D capable of digitizing analog signals at a maximum rate of 500 Msps. It runs on a single –5.2V supply and typically draws 2.8W power. It is supplied in a 68 lead ceramic LCC package.

(c) Very high resolution, low power (delta-sigma) A/Ds

Harris HI7190 24-bit, 15mW, CMOS A/D. The HI7190 is a 24-bit delta-sigma converter which offers 22-bit resolution with no missing codes. It operates from +/-5V supplies and typically draws 15mW (5mW in the standby mode). The part is offered in 20 pin plastic DIP and SOIC packages.

ADI AD7714-5 (24-bit, 5V), and **AD7714-3** (24-bit, 3V) <5mW CMOS A/Ds. The AD7714 is a 24-bit delta-sigma converter. It operates from a single supply (+5V for AD7714-5, or +3V for AD7714-3). The typical power levels are: 5mW (100uW in standby mode) for the AD7714-5, and 2.6mW (15uW in standby mode) for the AD7714-3. It offers 24-bit resolution with no missing codes. The part comes in 24-pin (plastic DIP, hermetic DIP and SOIC) and 28-pin (SSOP) packages.

Burr-Brown ADS1210 24-bit , 26mW CMOS A/D. The ADS 1210 is a 24-bit delta-sigma converter which operates from a single +5V supply. It typically draws 26mW (11mW in the sleep mode). It offers 24-bit resolution with no missing codes. It is available in 18-pin DIP and SOIC packages. Note: The evaluation results would also apply to ADS1211 which includes a 4-channel MUX. The ADS1211 is available in 24-pin (DIP and SOIC) and 28-pin (SSOP) packages.

(d) General purpose, low power A/Ds

Burr-Brown ADS7809 16-bit, 100kHz, 100mW CMOS A/D (with Latch-up protection circuit). The ADS7809 is a complete 16-bit 100kHz sampling A/D using CMOS-epi process. It operates from a single +5V supply, with power dissipation under 100mW. The part offers six analog input ranges: +/-10V, +/-5V, +/-3.33V, 0 to 10V, 0 to 5V, and 0 to 4V. It has serial output. As noted in footnote 8/ of the previous section, the latch-up protection circuit is under development at SEI.

PICO SYSTEMS ANTIFUSE SUBSTRATE RELIABILITY DATA AND OTHER ACTIVITIES

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The final report for the NASA/GSFC evaluation of the Pico Systems sea-of-antifuse substrate is available on the World Wide Web. It can be accessed from the Library in the Technology Validation Assurance homepage (http://misspiggy.gsfc.nasa.gov/tva/). Analysis of over twenty thousand device-hours of data, circuit plots, references and conclusions are available.

A number of other activities between NASA and Pico Systems are in progress. The antifuse substrate technology will be used as MCM substrate for a Space Technology Research Vehicle GSFC experiment (Principal Investigator: Ken Label/GSFC). NASA/Langley is currently in development of MCM utilizing an custom microcontroller (Principal Investigator: Jerry Tucker/LaRC). A low cost digital Command & Data Handling MCM is under development as an investigation in commercial tools and solutions (Principal Investigators: Harry Shaw, Robert Caffrey/GSFC). An in-depth investigation in single event effects on the antifuse substrate is ongoing (Principal Investigators: Ken Label, Richard Katz, Michele Gates, Henning Leidecker, Harry Shaw).

Additional investigations and applications are in the pipeline, including a collaboration with Army Research Labs, Johns Hopkins Applied Physics Labs and GSFC to evaluate high-g force capable MCMs (Principal Investigator: Larry Burke/ARL).

JPL SEE TESTS

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JPL has conducted two SEE tests-- one at Texas A & M (TAM) in January and another at Brookhaven National Laboratories (BNL) in March 26,1997. Several tests for "latchup only" were conducted at room temp:

ADI-AD7225TQ 8-bit DAC	No latchup at LET=87 MeV/mg/cm2
Harris HI1276 8-bit flash ADC	No latchup at LET=70
SPT SPT7725 8-bit flash ADC	No latchup at LET=120
Linear Tech LTC1419 14-bit ADC	No latchup at LET=120
National AD10262 12-bit ADC	Latchup threshold = 12
Samsung KM684002 4M SRAM	No latchup at LET=87

A test of the PIC16674A 8-bit microcontroller used to run the AD7225TQ DAC was very susceptible to latchup with LET threshold <<17 and latchup currents of several hundred mA.

A special latchup test of a Space Borne Inc. 32-channel autocorrelator also showed no latchup at LET=120 for a range of frequencies and voltages.

Two Interpoint DC/DC converters, MHF2805D and MHF2815D were tested in the "on" mode. There was no evidence of any SEE up to LET=94 MeV/mg/cm2.

In addition, there are some ongoing studies of the Intel 28F016SV & SA and the Samsung KM29N16000 flash memories.

For further discussion, please call Don Nichols at 818-354-5787 or FAX 818-393-4559.

ON-ORBIT OPTOCOUPLER ANOMALY

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The HST STIS instrument recently experienced an on-orbit anomaly with an optocoupler. This on-orbit anomaly has been attributed to the single event transient behavior of HCPL-5631 (6N134 family) optocouplers. The optocouplers are part of the STIS MAMA reset circuit. The anomaly causes a partial reset of the MAMA low voltage system. In all known occurrences to date, the processor has continued to operate normally, but two hardware registers were reset. The NICMOS instrument contains a similar circuit, and has experienced similar anomalies. The anomalies in both instruments have only occurred while HST was in the South Atlantic Anomaly (SAA) region.

The 6N134 family of optocouplers contains an LED and a high speed photon detector chip which uses a photodiode to detect the light signal from the LED. The manufacturer supplies several versions and packaging configurations for part type 8102802PA, used in the instrument. Some of the part types are listed in the following table.

Reliability Level	16 Pin DIP	8 Pin DIP	8 Pin DIP, Common V_{cc}, GND	16 Pin Flat Pack	20 Pad LCC
Commercial	6N134	HCPL-5600	HCPL-5630	HCPL-6650	HCPL-6630
Class H	6N134/ 883B	HCPL-5601	HCPL-5631	HCPL-6651	HCPL-6631
Class K	HCPL-268K	HCPL-560K	HCPL-563K	HCPL-665K	HCPL-663K
SMD	8102801	5962-9085501	8102802	8102804	81028032

Ground testing of HCPL-5631 optocouplers using 63 MeV protons has revealed that the protons produce transient pulses on the output of 20 to 60 nanoseconds duration. The high speed AC family logic parts used in the STIS MAMA reset circuit are sensitive to these short pulses. Similar testing on several other optocoupler types suggests that only fast optocouplers (bandwidth faster than 400 kbps) produce transient events. The length of the pulses seem to be inversely proportional (approximately) to the maximum measured bandwidth. No effort has yet been undertaken to determine the SET threshold (there is no SET threshold expected for a direct proton ionization event like this) or the effect of manufacturer, date code, or other factors. It should also be noted that no high-speed optocouplers using phototransistors were tested, however, the radiation effects group would expect to see similar transients on the outputs of those devices. The following results have been generated to date:

Manufacturer	Device	Speed	Transient Duration
Manufacturer "A"	5631	10 Mbps	20 to 60 nsec
Manufacturer "A"	5401	40 Mbps	20 to 25 nsec
Manufacturer "A"	4N55	400 Kbps	no transients
Manufacturer "A"	6N140A	400 Kbps	no transients
Manufacturer "B"	6N136	400 Kbps	no transients
Manufacturer "C"	4N48	400 Kbps	no transients

The effects of the anomalies on STIS will be mitigated by operational shutdowns during SAA passes and software modifications to detect any reset signals and force a complete reset of the MAMA. Corrective techniques for new builds include the addition of filtering capacitors or the use of redundant parts.

According to preliminary test data obtained by the GSFC Radiation Effects and Analysis Group, applications using fast optocouplers (e.g., 10 Mbps) that utilize photodiodes result in transients which can be expected on the outputs even if the devices are biased such that no light is being sent from the LED to photodiode (biased-off). These SEE related transients are on the order of < 1/bandwidth.

For slower optocouplers (e.g., 400 kbps) applications, no transients have been observed.

HERMETIC FEED THRU FIBER OPTIC CONNECTORS FROM G&H TECHNOLOGY

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G&H Technology, Inc. has a record of over 50 years at servicing the specialty connector market. G&H Technology Inc. is a supplier of interconnection solutions requiring advanced, high reliability electronic, electromechanical and mechanical components. Their reputation has been built and sustained in military, aerospace, undersea, mission critical industries and other hostile environments.

G&H Technology, Inc. has developed Fiber Optic Termini designed to fit standard size 16 cavities in the Umbilical Interface Connector as specified in Space Station specification SSQ 21637 (see Summary Background below for details). These termini are fully qualified to SSQ 21637. These termini are adaptable to Space Station connectors, SSQ 21635 (NATC, NZGL, NBLC, & NZGW), or other space-qualified D38999 fiber optic circular connector termini suitable for use in both hermetic and non-hermetic applications. Prototype units have already been tested to F-22 and Mil-C-38999 vibration levels (8 hrs vs. 3.5 min as required for Space Station). The new design by G&H incorporates several unique features, including a covered spring assembly, preform epoxy strength member capture, cable compatibility, and a simple alignment sleeve installation and removal tool. These new termini are grommet-safe by design!

Summary background on the SSQ space station connectors:

The SSQ 21635 ("General Specification for Connectors and Accessories, Electrical, Circular, Miniature, IVA/EVA Compatible, Space Quality") are a family of connectors designed for use in low earth orbits, satellite orbits and deep space missions with a life expectancy of 10 years minimum. The NSGL (NASA Zero-G Lever) and the NSGW (NASA Zero G Wing) are designed to be used in either external or internal vehicular (vacuum and pressurized environments). These connectors are designed to be taken from one environment to another and are considered to be "user friendly" to an astronaut even when suited for extra-vehicular activity. The NBLC (NASA BreechLok® Coupling) and NATC (NASA Threaded Coupling) connectors are designed for low to no astronaut interfacing. They are intended for use in non repairable satellites or deep space probes. The SSQ 21637 connectors are of the same classification as the SSQ 21635, however the NU (NASA Umbilical) connectors are designed for umbilical interfacing with an orbital replacement unit or mechanized mating device. These connectors are not designed to be mated by hand in any environment. Although these specifications discuss requirements for only the electrical connector bodies the contact termini can either be electrical or fiber optic.

If you have an immediate or pending future interest in this new fiber optic termini design, offering improved design characteristics, please contact Gene Taylor at G & H Technology, Inc. of Camarillo, CA (805) 484-0543 or (805) 389-5766. Also if you feel your project could make use of these termini in a future application but still have questions feel free to call.

PROGRAMMABLE LOGIC APPLICATION NOTES

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This column will be provided each quarter as a source for reliability, radiation results, NASA capabilities, and other information on programmable logic devices and related applications. This quarter's column will differ from previous editions; there will be a small section on some topics of interest and then two summary reports on programmable logic devices. The report on the Chip Express Laser Programmable Gate Array expands on data in the last issue. Also, preliminary testing has been completed on the Actel A32200DX, a 20,000 gate FPGA; the A32140DX device with 14,000 gates will be tested in July My apologies for not being able to complete the usual article in time to meet the deadline; please give me a call or e-mail if additional information is needed. The topics of interest will be expanded on in the next edition of EEE Links.

Topics of Interest

- Additional testing of A1020B has been completed. The latchup thresholds have decreased from earlier versions.

- No latchup was detected in the RH1020, a derivative of the A1020B.
- Some modern FPGA devices are packaged in a cavity down configuration (i.e., some Xilinx devices, A1460A and A14100A in CPGA's). Check your package and thermal analysis.
- In the 3200DX family, to disable the JTAG circuitry, remove the restriction on JTAG pins; there is no 'disable JTAG button.'
- When using C-Module flip-flops in Act 3, for example, the analysis software will not automatically calculate external setup and hold times. C-Modules are used in this application since the I/O-Module flip-flops are SEU soft. Actel has sent in a procedure for automating these calculations.
- Running out of flip-flops in Act 3 designs? These devices with a large number of I/O pins have two flip-flops per I/O module that can be used for functions such as shift registers. These unused pins can be utilized without adding any traces to the PC board.

Acknowledgements and References

NASA/GSFC - Ken LaBel
(http://flick.gsfc.nasa.gov/radhome.htm)
Actel Corp.: JJ Wang
Gary M. Swift : California Institute of Technology/Jet Propulsion Laboratory
Martha O'Bryan, Hughes STX

EVALUATION OF THE CHIP EXPRESS QYH580 (LPGA)

Test Date: February, 1997, March, 1997, May, 1997

Test Location:
Brookhaven National Laboratory (Heavy Ion)
NASA/GSFC (Total Dose)
NASA/GSFC (DPA)

Test Device: Chip Express QYH580

Prepared By: NASA/GSFC

INTRODUCTION

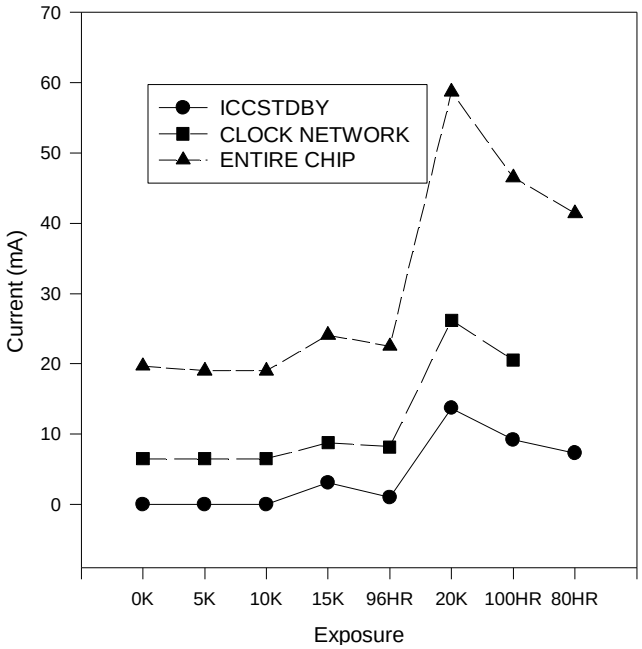
The QYH580 is a member of the Chip Express QYH500 family. This family is a 0.8 μm bulk CMOS technology. The QYH500 gate array can be configured to yield up to 60,000 usable "gate array gates". This technology utilizes two types of cells: I/O cells and 2 input NAND gates. The I/O cells may be programmed into a variety of configurations; however, there is no storage available in these cells. The two input NAND gates can be configured to provide buffers, logic functions, or flip-flops. The I/O structure is flexible and the devices may have the pins configured per user specifications. For this evaluation, the QYH580 was configured to be pin compatible with an Actel A1280A in a CPGA176 package for both a proof of concept and compatibility with existing test infrastructure. Chip Express is foundryless; the QYH500 series of devices is fabricated by Yamaha.

The QYH500 series is a channeled gate array architecture. Metal routing segments are "pre-placed" in the channels and all possible connections are made during integrated circuit fabrication. The chip is "programmed" by selectively opening connections leaving the interconnect in a state which implements the design netlist. This is opposite of antifuse-based Field Programmable Gate Array (FPGA) technology where connections are made during programming by making an antifuse into a conductor. Note that only a small fraction of possible connections are needed in a gate array; thus in an FPGA a small number of connections must be programmed and in the QYH500 the majority of connections must be made into open circuits.

The QYH500 series, for the purposes of this evaluation, can be programmed using two different techniques for the identical base arrays. The first technique utilizes a laser to remove the unwanted connections and takes on the order of 1 hour at the factory. Turn around for these *Laser Programmable Gate Arrays* (LPGA) is on the order of days. A *one mask* technology can remove metal connections from the base array on two levels of metal using a single masking step. In both cases, unused routing segments are left floating. For quick prototypes (as were our test devices) the LPGA is used and the device is not passivated. The 883-qualified devices are processed using one mask technology and are passivated following processing. The devices are qualified for both V_{CC} = 3.3 and 5.0 volts.

This evaluation is considered preliminary: 3 devices were

QYH500 LPGA1 TID TEST



used for heavy ion testing, 1 for total ionizing dose (TID) testing, and several unprogrammed devices were used for a quick, coarse, destructive physical analysis. The sample device utilized approximately 35,000 gate array gates, roughly 4 times that of our A1280A 1.0 µm samples. It was observed even with the higher gate counts, the dynamic power of the QYH500 was less than the A1280A; static power was essentially 0 uA (our system, as configured, had a measurement resolution of 10 µA).

The CX2000 series of devices is a 0.6 mm epi-layer technology fabricated by Tower Semiconductor. This part will be evaluated in future tests (July, 1997).

TOTAL IONIZING DOSE TEST

TID testing was performed at NASA/GSFC using a Co-60 source. The device was statically biased at V_{CC} = 5.0 VDC with all inputs terminated to ground. The dose rate was 5 krads (Si) / day or 0.058 rads (Si) per second. Functional tests were run at each radiation step of 5 krads (Si) and three device current parameters were measured: standby (the entire chip static), clock on (measuring the clock distribution network), and dynamic, with all elements toggling at approximately 500 kHz.

No functional failures were detected and a plot of I_{CC} vs. radiation and annealing is given below. Testing proceeded to 20 krads (Si). All annealing was biased at V_{CC} = 5.0VDC and was at room temperature.

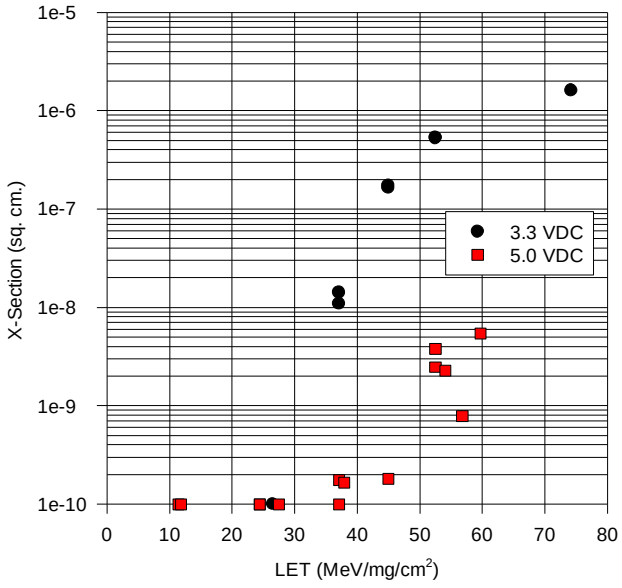
HEAVY ION TESTING

Heavy ion Single Events Effects (SEE) testing was performed at Brookhaven National Laboratory. The device was monitored for single event upset (SEU), single event latchup (SEL) and device functionality. Strip charts were made of I_{CC} vs. time. Nominal fluence for each run was either 0.5 x 10^7 or 1x10^7 ions/cm^2. Runs were performed with V_{CC} either in the standard 5.0 VDC ± 10% range or in the 3.3 VDC ±10% range.

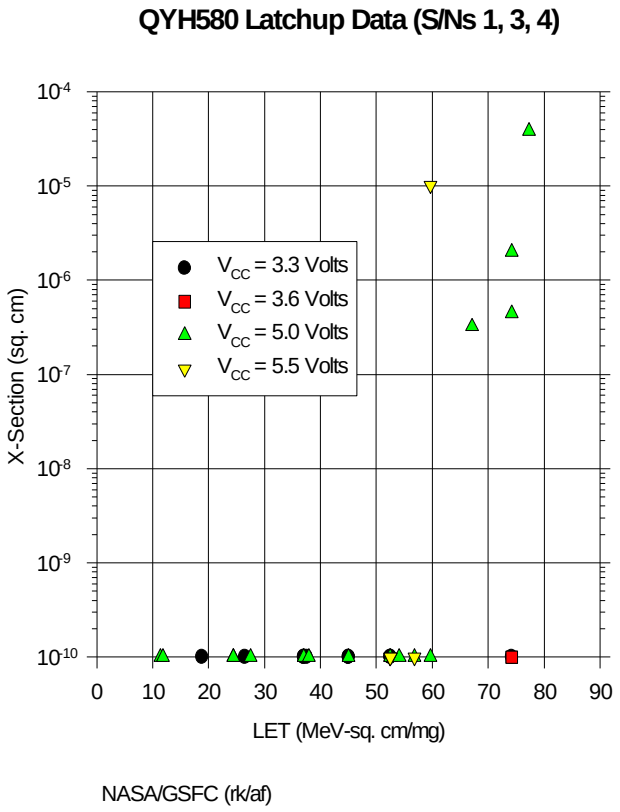
No functional failures were observed during testing. Latchup was detected at relatively high LETs with V_{CC} in the 5.0 VDC ± 10% range; no latchup was observed in the lower voltage range up to an LET of 74 MeV-cm^2/mg. Latchup data is summarized in the chart below. SEU performance was very good with upsets first detected near LET = 40 MeV-mg/cm^2 with a very small cross-section; the SEU performance is also summarized in a chart below. SEU performance has been measured for both 5.0 and 3.3 volt bias levels. The good SEU performance is believed to come from the relatively high capacitance of the "pre-laid" metal routing segments. Note that this performance is similar to that observed for Actel C-Module flip-flops in one of it's two storage states which uses a similar routing segment scheme.

Points on the graphs at the 1x10^{-10} line indicate that no SEE was detected for that run.

QYH580 SEU Data (S/Ns 1, 3, 4)



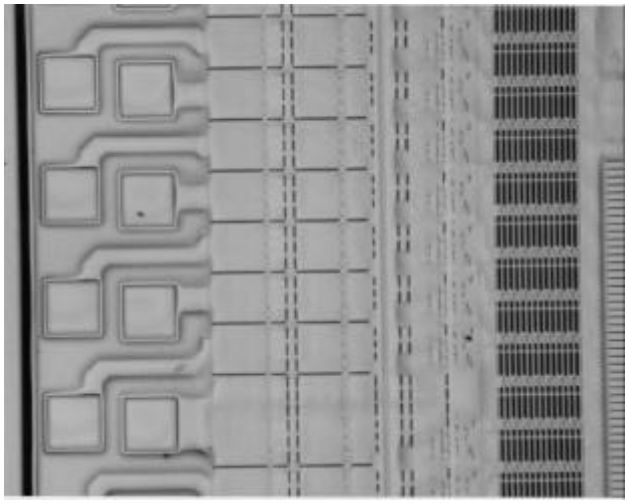
NASA/GSFC (rk/af)
June 6, 1997



DESTRUCTIVE PHYSICAL ANALYSIS

Unprogrammed devices from the QYH500 and CX2000 series were subject to a quick, rough, destructive physical analysis. No obvious defects were noted and the preliminary evaluation showed processing consistent with 883 standards. Fully processed samples are expected for a more thorough analysis in the near future.

The CX2000 series has a very high I/O pin count. Note, in the photograph below, that many of the I/O pads are staggered. This can have implications for package selection and chip on board (COB) or multi-chip modules (MCMs).



File: 103x2200.bmp

Software and Design Flow

Chip Express has two families for low volume applications using it's LPGA and OneMask technologies; the QYH500 is 0.8 micron, two level metal and the CX2000 family is 0.6 micron, three level metal. The “golden” simulator for both parts is Cadence Verilog XL. Also supported for signoff are Synopsys VSS and Model Tech's V-System with the VHDL flow utilizing Vital-95. Synthesis for these devices is provided by Synopsys' Design Compiler and Exemplar Leonardo. Scan insertion is accomplished using either Synopsys' Test Compiler or Syntest's Picasso. Motive is used for static timing analysis.

For the QYH500 family only, Viewlogic schematic capture and simulation (ViewDraw and ViewSim) are supported.

PRELIMINARY HEAVY ION EVALUATION OF THE ACTEL A32200DX FIELD PROGRAMMABLE GATE ARRAY

Test Date: May, 1997

Test Location:
Brookhaven National Laboratory

Test Device:
A32200DX, TD32200 Pattern

Foundry: Chartered

Lot Codes:
ACQ03818.1/456157, ACQ06719.1/497634

Prepared By:
NASA/GSFC (R. Katz, A. Feizi),
Actel Corp. (J.J. Wang)

INTRODUCTION

The A32200DX is part of the Actel Integrator Series of FPGAs that consists of the A1200XL products as well as the A3200DX products. The A1200XL devices are derived from and share a user architecture with the more familiar A1200A series parts, such as the A1280A which has been heavily tested by NASA and the aerospace industry. The A3200DX family shares the same C-Module and S-Module 'logic diagram' with the A1200 series; the I/O-Module structures are also similar but differ with the addition of JTAG 1149.1 capability in some A3200DX products.

The A3200DX family introduces new architectural features. These include larger capacity (higher gates available, wide fan-in decode modules, dual-port SRAM, higher I/O counts, IEEE JTAG 1149.1 support, and 4 low-skew quadrant clocks.

The A32200DX has the following capabilities:

- 20,000 Gates (not including SRAM).
- 10 dual-port SRAM modules, 256 bits each.
- 6 Clocks.
- 202 User I/O.
- JTAG Capability (w/out the optional hard reset to the TAP controller).

DUT and TEST DESIGN

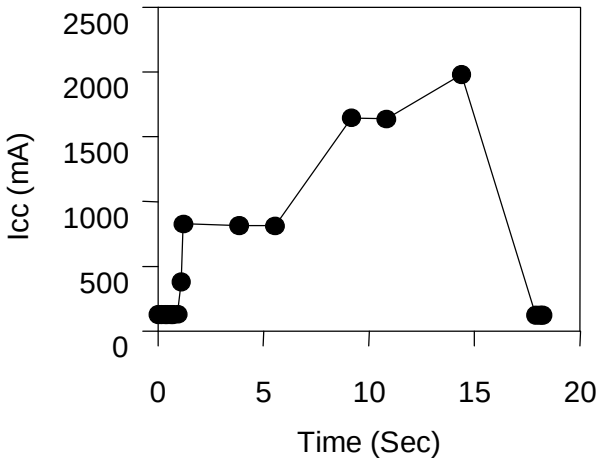
The DUT design used for this evaluation is called the TD32200 and was originally intended for total dose testing of this device. It includes the usual test structures such as flip-flops, gates, counters, shift registers, etc. Additionally, it utilizes the quadrant clocks and the SRAM bits. The design has a built-in-test (BIT) capability for the SRAM where different patterns are successively written to and read back/checked from the SRAM. Internal monitors are available showing that the BIT is running and error pulses are output whenever a SRAM error is detected. This design pattern had the JTAG feature enabled.

The test set consisted of a custom test fixture which provided the ability to start/stop clocks, reset the device, test all functions, provide monitors and output error pulses. During a SEE run, the error monitor is run into a counter; after a test run, the entire functionality of the DUT is verified. Additionally, strip charts are made of I_{CC} vs. time.

For this test, the DUT is packaged in a PQFP208 package. The device has a 10 μm epi-layer, common to all Actel commercial and military devices. These samples, from two different date codes, were manufactured at the Chartered foundry.

TEST RESULTS SUMMARY

Initial exposures used 290 MeV Bromine, with an LET of 37 MeV-cm^2/mg and a range of 37.3 μm with normal incidence. All 4 runs with S/N 001 appeared to latch with high currents. The average latchup cross section was > 3.7×10^{-5} cm^2. S/N 002 behaved similarly. A sample strip chart of I_{CC} vs. time is shown below. S/N 001 was also exposed to 265 MeV Nickel, with a LET of 27 MeV-cm^2/mg and a range of 42.2 μm with normal incidence. The device quickly latched.



A32200DX Latchup Current Strip Chart

ANALYSIS AND FUTURE WORK

The initial suspect for the cause of latchup was the SRAM modules; this is the key new technology that is

in the A3200DX family. Previous SEE testing on the A1200XL series (both 0.6 and 0.8 μm) showed no sign of latchup. An examination of the SRAM circuit layout did show that there were no guard rings. The next round of tests will include the same TD32200 pattern with the JTAG circuitry disabled and a similarly configured A32140DX; this device does not have the SRAM modules. Lastly, the failed DUTs have been sent to failure analysis for verification of epi-layer thickness.

FIELD PROGRAMMABLE GATE ARRAY (FPGA) TECHNOLOGY PROTOTYPE

Test Location: Brookhaven National Laboratory (Heavy Ion), Indiana University (Proton), NASA/GSFC Bldg. 22 (Total Dose)

Test Device: MKJ911, KJ911

Prepared By: NASA/GSFC (R. Katz)

INTRODUCTION

The MKJ911 and the KJ911 devices represent technology prototype Field Programmable Gate Arrays. While similar in respect to previous antifuse-based devices on the market, they have significant new technologies and architectural features; these are applicable both to commercial and space-borne applications. This report will review some of these key technologies, their relevance to space-based applications, and a preliminary radiation evaluation. Certain details such as gate count capability are omitted, as they are considered by the manufacturer to be competition sensitive and do not affect this study. The MKJ911 and the KJ911 are internal code names for these technology prototypes.

Most FPGA's have used a channeled gate array architecture; that is, routing resources were located mainly in the channels in between rows of logic modules. For SRAM-based FPGAs, this is necessary since the memory elements and pass transistors need a substrate for the fabrication of transistors. These, combined with the routing segments, account for ~ 50% of the area of an FPGA. For the Actel dielectric antifuse (ONO – oxide nitride oxide), a channeled architecture was also used; the antifuses use the substrate for one terminal and polysilicon for the other. While in principle the antifuse can be fabricated between two layers of polysilicon, it is not practical to do this. Additionally, certain pass transistors need to be fabricated for testability and programming structures. Typical resistances of the dielectric antifuse are between 300 and 500 ohms. First generation Quicklogic devices also used a channeled architecture with the metal-to-metal antifuse.

Two key technologies, among others, permit an improvement in FPGAs: three layer metal processes and the metal to metal antifuse. These two technologies permit antifuses to be fabricated 'on top' of the logic modules, drastically cutting the size of the die and making parasitic capacitances less, improving speed. Additionally, the metal to metal antifuse has a typical resistance of 25-50 ohms and a lower capacitance than dielectric antifuses, also improving routing speed. On the negative side, the metal to metal antifuses have higher leakage currents than their dielectric antifuse cousins.

An additional benefit of the metal to metal antifuse is its lower programming voltage (for FPGAs and PALs); this is typically 10-11 volts as compared to the 18-20 volts for dielectric antifuse products. This makes the construction of high voltage transistors simpler and permits the use of thinner epi-layers. The high voltage of the Actel RH1280, for instance, limited the epi-thickness to 5 μm; the KJ911 has been fabricated with 2 μm epi.

Additionally, the MKJ911 and the KJ911 have significant architectural improvements over previous generation metal-to-metal antifuse products and dielectric antifuse devices; these are not discussed here, as the information is not yet released.

DUT and TEST DESIGN

Two different DUTs are used; both are identical FPGA designs and have identical patterns. The pattern used is called BURN, which was designed for testing of the silicon technology. The MKJ911 device is fabricated at Matsushita and has a 10 μm epi-layer; the KJ911 is fabricated on Lockheed-Martin's radiation-hardened line and uses a 2 μm epi-layer. All devices are in a PQFP208 package.

The test of the device uses the 'emulated gold chip' approach. An Actel A1020 has device stimulation capability, error detect capability, built-in-test (BIT), and a gold chip emulation of the (M)KJ911. If an error is detected, it is classified as one of three types, depending on the chip section and state, and error pulses are put out on one of three corresponding lines. In the event of an error, the A1020B will reset both the DUT and the emulated DUT and they will resume operation in lock step. The structure of this design (BURN), which consists of structures designed to check IC reliability, results in an error count that is biased slightly high; the cross-sections reported here should be considered an upper bound.

In addition to monitoring for SEU's, the power supplies' currents are monitored. These devices use a 3.3 VDC supply for the logic core and are capable of mixed voltage

I/O. For these evaluations the I/O modules were configured in 3.3 volt, 5 volt-tolerant mode.

Lastly, the as tested configuration had the IEEE JTAG 1149.1 port enabled; the optional hard reset for the TAP controller is not implemented on these prototypes.

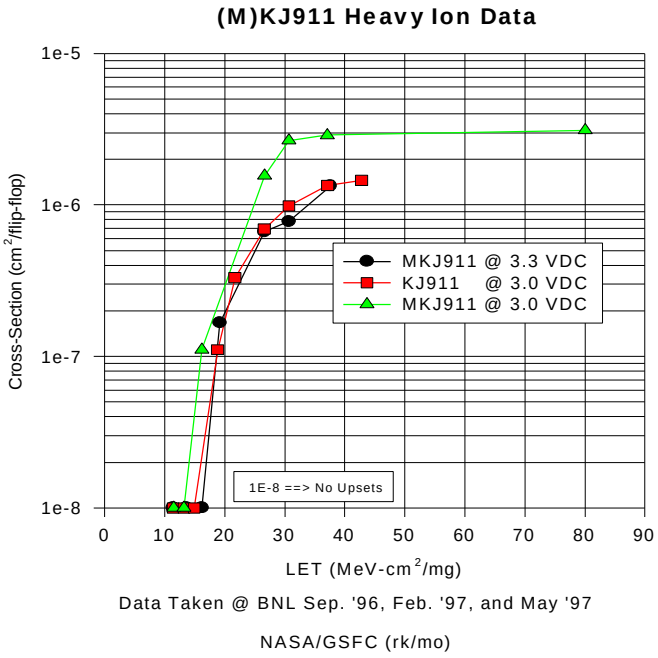
The identical test configuration is used for heavy ion, proton, and total dose testing. All DUT card I/O is buffered with RS-422 drivers and receivers. For total dose testing, the support IC's are shielded and the DUT is configured with a static bias.

The DUT and the support IC's and are located on independent power supplies.

TEST RESULTS SUMMARY

Three types of tests were run: heavy ion, proton, and total ionizing dose.

Both of the device types, MKJ911 and KJ911 were tested for heavy ion SEU susceptibility. They both showed a similar upset threshold; the lowest LET where upsets were detected was 18.8 MeV-cm^2/mg for the 2 µm epi KJ911 and 13.2 MeV-cm^2/mg for the 10 µm epi MKJ911. Additionally, both devices appeared mildly susceptible to upsets that resulted in a loss of functionality and a change in supply current (both up and down). It is suspected that these were upsets in the JTAG TAP controller. The SEU results are summarized below. Note that for these samples, the 2 µm epi-layer parts had a smaller cross-section than the 10 µm epi-layer devices, for equal supply voltages.



Note: MKJ911 fabricated at MEC w/ 10 um epi
KJ911 fabricated at L-M w/ 2 um epi
Cross Sections are an upper bound;
DUT pattern limited instrumentation.

The MKJ911 was tested at the Indiana University cyclotron with 196 MeV protons. No upsets were detected. An I_{CC} vs. dose strip chart is included on the following page. This commercial device (MEC foundry) showed good total dose performance; after 50 krads (Si) exposure in a short period of time, the supply current increase was still relatively moderate. Part-to-part and lot-to-lot variance in total dose performance for this commercial foundry has not yet been determined.

Lastly, devices are being total dose tested in the NASA/GSFC Cobalt-60 cell. To date, a device from the Lockheed-Martin foundry has accumulated 200 krads (Si) at a dose rate of 2 krads (Si) per hour; no degradation of the device has been observed (i.e., no changes in the device supply currents, static and dynamic) and the device passed functional testing.

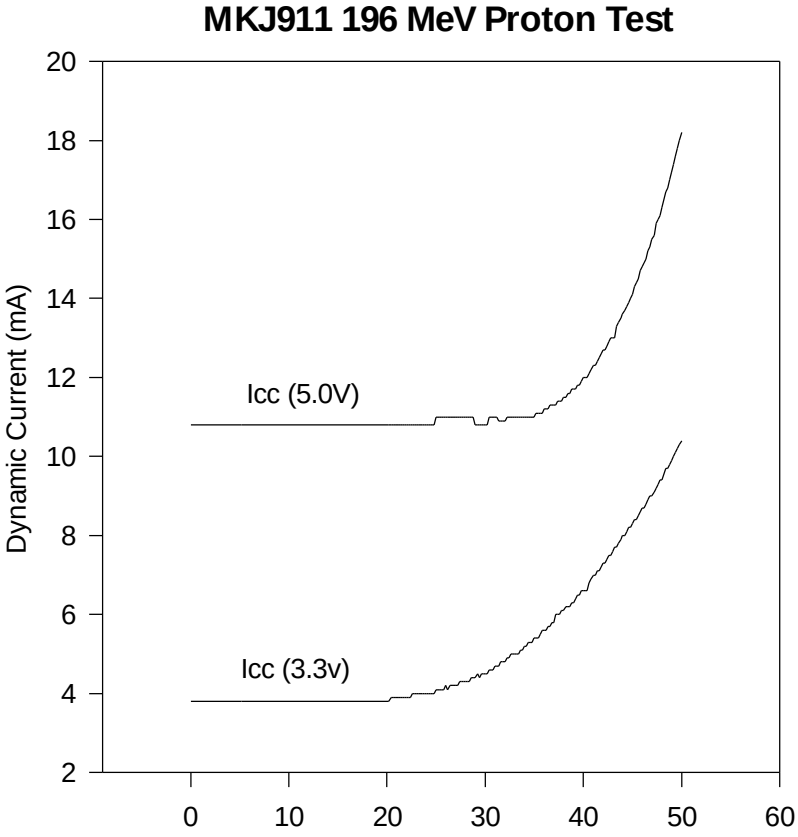
CONCLUSION AND FUTURE WORK

Further work is planned for the (M)KJ911 series. This includes heavy ion tests with higher LET ions, additional proton tests, and a more in-depth TID study. Additionally, leakage current performance as a function of temperature will be investigated. Prior to the completion of these tests, a new test pattern will be put into the (M)KJ911 series, designed specifically for radiation, performance, and reliability evaluations.

The MKJ911 has the potential to make a high-speed radiation-tolerant FPGA. The SEU threshold of approximately 13 MeV-cm^2/mg at V_{CC} = 3.0 volts is 'moderate' but far superior to the performance of S-Module flip-flops in other Actel devices running at higher supply voltages, which is the current base line for many missions. For the high speed applications this device is designed for, the 3.3 VDC core voltage will be critical for maintaining reasonable power dissipation levels. The device has shown immunity to proton upset with 196 MeV protons, a problem with the A1280XL series devices (including the RH1280) and the 0.8 µm Act 3 family (A1460A, A14100A), for example.

The KJ911 improves upon the performance of the MKJ911; this is believed to be primarily the result of the processing at the Lockheed-Martin facility. The use of the 2 µm epi-layer may contribute to the lower SEU cross-section and higher upset threshold of the KJ911 as compared to the MKJ911; however, for SEU performance, the device is still considered radiation-tolerant. Total dose capability, however, is in the radiation-hardened class. Currently, the KJ911 is the overall hardest FPGA of any that we have tested to date.

The KJ911's sea of gates architecture results in a decreased die size relative to a channeled gate array architecture. This, combined with the circuit design internal to the KJ911, should make the device amenable to SEU-hardening while maintaining a relatively small die size and good electrical performance.



Total Fluence = 810 x 10^9 protons/cm^2

Zero upsets over the course of the test.

FILE = C:\USER\RESEARCH\NOV-96.IND\MKJ911.SPW

rbk 11/21/96

JET PROPULSION LABORATORY
PARTS ANALYSES

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Failure analyses (FA), destructive physical analyses (DPA), and part constructive analyses (CPA) have been performed on the following part types. For a copy of the report, contact me (phone 818-354-9529, fax 818-393-4559 or e-mail to joan.c.westgate@jpl.nasa.gov) and request the desired document by "Log#".

FAILURE ANALYSIS

Log No.	Manufacturer	Date Code	Part Type	Part Number
6710	CTS	9423	Solid State Power Switch	10137607
6734	Teledyne	9537	Hybrid	2301670-314
6735	Motorola	9524 9243	D-Flip-Flop NOR Gate	10H131 10H502
6736	Kemet	9511	Ceramic Capacitor	CKR06, 2nFd
6764	Genicom	9440	Relay (4PDT)	3SBM
6767	Linear Technology Corp.	1C030	Operational Amplifier	RH108AH
6789	Solid State Devices	9243	Silicon Controlled Rectifier, 25 Amp	ST12127-DON688SR
6790	Teledyne Relays	9410	DPDT, Non Latching Relay	K412V
6802	Teledyne	9537	Hybrid	2301670-314
6845	Sertech	9520	Dual Rectifier Diode	DK4929
6847	PMI	4D9450E	Quad Operational Amplifier, Op-400	5962-8777101MCA
6858	Actel	9224	Field Programmable Gate Array	A1020 HFR
6867	Marconi Electronic Devices Harris Harris	0324 9309A 9302A	Hex Inverter Dual-D Flip-Flop with Set and Reset Quad 2-Input Exclusive-OR Gate	54HCS04 54HCS74 54HCS86
6871	Mitsubishi	9522	4Mbyte DRAM	M5M44100A
6833	BKC Semiconductor	9512	Diode, Fast Recovery	JNTXV1N5806

DESTRUCTIVE PHYSICAL ANALYSIS

Log No.	Manufacturer	Date Code	Part Type	Part Number	Result
6782	Powerex	9311B	Silicon Controlled Rectifier	JTX2N1777A	F
6848	SSDI	None	PNP Transistor	2N2605	F
6857	Powerex	8721	Silicon Controlled Rectifier, 7.4Amp	ST12126-D1777ASR	P
6859	GE	7942, 8343	Silicon Controlled Rectifier, 7.4Amp	ST12126-D1777ASR	P

PART CONSTRUCTIVE ANALYSIS

Log No.	Manufacturer	Date Code	Part Type	Part Number
6746	Linear Technology	9524	Step Down Switching Regulator	LT1076CT
6747	Linear Technology	9530	100khz, 1.25A High Efficiency Switching Regulator	LT1172IN8
6748	Linear Technology	9512	Step Down Switching Regulator	LT1176CN8
6749	Linear Technology	9330, 9543	Micropower, DC/DC Converter	LT1111CN8
6750	Linear Technology	9613	Dual, Very Low Power, High Speed OP-AMP	LT1352CN8
6751	Linear Technology	9625	14 Mhz, 7V/µS, Single Supply, Dual Precision OP-AMP	LT1211CN8
6752	Linear Technology	9338C	High-speed, Current Mode, Pulse Width Modulator	LT1243IN8
6753	Linear Technology	9532	250 kHz, Low Supply Current, High Efficiency, 1.5A Switching Regulator	LT1373CN8
6754	Linear Technology	9440, 9521	Complete Single Supply, 12-bit, Voltage Output DAC	LTC1257IN8
6755	Linear Technology	9537	Dual Micropower, Zero Drift, OP-AMP with Internal Capacitors	LTC1047CN8
6756	Linear Technology	9624	14-bit, 800Ksps, Sampling ADC with Shutdown	LTC1419CS

GODDARD SPACE FLIGHT CENTER PARTS ANALYSES

Listed below are the EEE parts analyses completed by the GSFC Parts Analysis Laboratory. The GSFC reports are available to NASA personnel and current NASA contractors by contacting your NASA project office.

CA jobs						
Job Number	**Manufacturer**	**Date Code**	**Part Type**	**Part Number**	**Result**	**Date**
78165	AVX	9714A	capacitor	87106-085	P	5/8/97
78075	NES	9610	transistor	JANTXV2N2907A	F	3/6/97
78150	Silicon Transistor Corp.	9134	transistor	JANTXV2N6351	F	4/30/97
78147	National Semiconductor	9524A	microcircuit	54ACTQ541DMQB/QC	P	4/28/97
78141	BKC Semiconductors Inc.	9702	diode	JANTXV1N6642	P	4/23/97
78154	National Semiconductor	9650	microcircuit	M38510/75701BCA	P	4/30/97
78155	National Semiconductor	9638	microcircuit	M38510/75302BCA	P	4/30/97
78133	National Semiconductor	9441	microcircuit	5962-8875501EA	P	4/15/97
78140	BKC Semiconductors Inc.	9704	diode	JANTXV1N6638	P	4/23/97
78138	NES	9640	transistor	JANTXV2N2907A	P	4/21/97
78153	Optek Technplogy Inc.	9644	optically coupled ins.	JANTXV4N48	P	4/30/97
78136	National Semiconductor	9549A	microcircuit	54ACTQ541DMQB/QC	P	4/21/97
78134	Compensated Devices Inc.	9641	diode	JANTXV1N5822	F	4/15/97
78097	National Semiconductor	9709	microcircuit	M38510/75302BCA	P	3/24/97
78132	Dale Electronics	9712	Resistor	M8340106K59ROJG	P	4/16/97
78063	Electronic Designs Corp.	9642	microcircuit	5962-8959829MYA	F	2/14/97
78151	Semtech Corp.	9417	diode	JANTXV1N5615	P	4/30/97
78152	Microsemi Corp.	unknown	diode	JANTXV1N4958	P	4/30/97
78061	JDI	9705	capacitor	87106-085	F	2/24/97
78086	Optek Technplogy Inc.	9535	Hall Effect Sensor	OMH090B	F	3/17/97
78123	Semtech Corp.	9712	diode	SET010211	P	4/8/97
78044	Unitrode	9548	microcircuit	UC1717SP/883B	P	2/18/97
78090	Lockheed Martin	9643	microcircuit	167A690-346	P	2/28/97
78080	National Semiconductor	9421	microcircuit	M38510/75307BEA	F	3/13/97
78017	Dale Electronics	9625	resistor	M8340106K1001JC	F	2/6/97
78052	Lockheed Martin	9647	microcircuit	5962H9215303QNC	F	2/24/97
78093	Lake Shore Cryotronics	9706	diode temperature sensor	DT470SD13	P	3/18/97
78029	National Semiconductor	9619B	microcircuit	5962-8777801XA	P	2/14/97
78033	Semicon Inc.	9610	diode	JANTXV1N5639A	P	2/7/97
78034	Analog Devices	9623S	microcircuit	AD590KF/883B	P	2/10/97
78023	Teledyne	96351	relay	M39016/12-058M	P	2/19/97
78040	Dale Electronics	9233	Resistor	M8340106K47ROGG	P	2/12/97
78015	Dale Electronics	9625	Resistor	M8340102K1000FA	P	2/7/97
78001	Intel	9451	microcircuit	MG80486DX266	P	1/27/97
78021	National Semiconductor	9544	microcircuit	M38510/75711BRA	P	2/6/97
78026	AMD	9615	microcircuit	5962-8605305LA	P	2/6/97
78016	Microsemi Corp.	9631	diode	JANTXV1N6642	F	2/10/97
78027	Motorola	9606	transistor	JANTXV2N2905A	P	2/14/97
78037	Microsemi Corp.	9611	diode	JANTXV1N6638	F	2/11/97
78022	Microsemi Corp.	9125	diode	JANTXV1N6312	P	2/12/97
78045	Microsemi Corp.	8003	diode	JANTXV1N2809RB	F	2/20/97
72031	Teledyne Electronic Techn.	9623	hybrid	G311P782	F	1/6/97
78010	Teledyne	9439	relay	422K-0162	P	2/4/97
72041	Interpoint	9646	hybrid	5962-9319301HXC	F	1/15/97
78006	CDI	9528	diode	JANTXV1N5711-1	P	1/31/97
78007	CDI	9610	diode	JANTXV1N5529B1	P	1/31/97
72037	XICOR	9536	microcircuit	X28VC256EMB-55	P	1/22/97
72033	McCoy	9610	hybrid	M55310/19-B11A16	F	12/11/96
72036	Interpoint	9642	hybrid	5962-9316301HXC	F	1/6/97
72026	Lockheed Martin	9643	microcircuit	167A690-346	P	11/27/96

FA Jobs						
Job Number	**Manufacturer**	**Date Code**	**Part Type**	**Part Number**	**Result**	**Date**
72014	SM	Jul-96	Motors	342671	Dimensions	4/8/97
72035	Motorola	8908	Transistor	JTXV2N2857	ESD	2/7/97
78009	Analog Devices	9550	Microcircuit	5962-932091	Radiation	3/18/97
78011	Harris	9424	Microcircuit	M38510R0553	Unconfirmed	3/3/97
78014	SEI	9512	Quad Transistor	SD5000	ESD	2/5/97
78058	Harris	9249	Microcircuit	HCS273	EOS/ESD	3/14/97
78103	IIZ	9336	Hybrid	BUS-65142-616	Corrosion	4/18/97
78109	Cal-logic	9633	Quad Transistor	SD5000	Marginal	4/4/97

EV Jobs						
Job Number	**Manufacturer**	**Date Code**	**Part Type**	**Part Number**	**Result**	**Date**
71412	Isotek	H22	Shunt Resistors	SMV-R0039	?	5/15/97
78004	Eagl Picner	Various	Battery Cells	SZHR1.5	?	3/28/97
78046	Loral	Oct-96	Hybrid	292045-N2	?	3/21/97
78130	HunterStanley	9615	Capacitor	3045	?	4/16/97

GIDEP & NASA ADVISORY IMPACT REPORT

NASA Advisories, GIDEP Alerts, Problem Advisories, Safe Alerts, Product Change Notices, Diminishing Source Notices and Agency Action Notices Related to EEE Parts

GIDEP & NASA Advisory Impact Report summary will no longer be included in the EEE Links publication. For the most current information on parts issues please refer to the EPIMS database on the WWW. The URL for EPIMS-WEB is : http://epims.gsfc.nasa.gov

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